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8th Annual End-of-Life Directory

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Volume 9 Number 3 March 2007 www.cotsjournalonline.com

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COM 3	RS–232	NA	RS–422/485
COM 4	RS–232	NA	RS–232
COM 5	RS–232/422/285	NA	NA
COM6	RS–422/485/TTL	NA	NA
LPTI	0	0	1
EIDE	2	2	1
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COTS JOURNAL

Features

March 2007 Volume 9 Number 3

Departments

Coming in April...
...See Page 69

Special Feature

PC/104 in the Military

Tech Recon

Switched Fabrics

System Development

Annual EOL Directory

Technology Focus

FPDP I&II and Serial FPDP Boards

COTS View

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Cover Story ..... Page 14

Maj. Gen. Fred D. Robinson, 1st Armored Division commanding general, and Col. John RisCassi, commander of 2nd Stryker Cavalry Regiment, review troops from a Stryker Infantry Carrier Vehicle during a welcome ceremony in Vilseck, Germany last fall. The Stryker ICV has an FBCB2 digital communications system that allows communication between vehicles—and up to battalion—through text messaging and a map network. The map shows the position of all vehicles on the battlefield. Under development for the Stryker is a new Power and Data Management Architecture (PDMA) to support future upgrades and improvements.

Photo Courtesy of U.S. Army by Spc. Andrew Orillion

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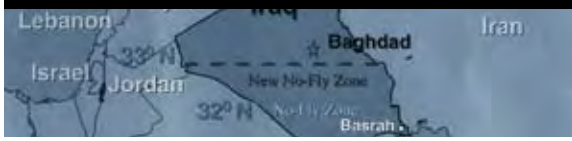

Keeping the Tech Plate Spinning

Sooner or later—I'm hoping not too late—our government has to start dealing with the reality of defense. When I was in fourth grade learning about the States, the revolutionary war and the establishment of the federal government, the reason for States conceding to have a federal government was for a unified defense. That was first and foremost. Now first and foremost our federal government sees its purpose as ensuring that the politician's club stays solvent and that each of its members stays as long as they want. And that after they leave the club they get a good alternate opportunity. Defense? Well, they can juggle that and use it as they need to in order to be part of the club.

Now that the federal government has put its fingers in so many issues surrounding our lives, it reminds me of watching a juggler that is juggling balls and spinning plates. All he can do is run from one plate to another and throw the balls ever higher. Eventually something has to "give," especially if you're bent on continuing to add plates or balls. What is "giving" right now is our technology. Politicians must have forgotten that leading-edge technology and our ability to fund its development ended the cold war. Technology is what we are focusing on to keep the number of warfighters we need to an absolute minimum and to keep them as much out of harm's way as we can. Face it. All our leading-edge technology is key to our defense.

ITARs (International Traffic in Arms Regulations) supposedly control the distribution of sensitive material to foreign powers and companies. A few years back we had to do some severe arm-twisting of Israel not sell arms to China that contained sensitive technology. More recently I read that Boeing declined to bid the Apache Longbow helicopter for a requirement out of Turkey because Turkey required a transfer of technology that was in violation of U.S. export controls. But, Boeing does have an alternative approach to providing Turkey Apaches through a Foreign Military Sales (FMS) scheme. Huhhh……?

Don't get me wrong, but having to deal with ITARs in the past regarding standard COTS subsystems was a real pain. It was an unending exercise to examine technology that was common knowledge worldwide. I get the feeling our government may have lost focus and forgotten that the original objective for establishing ITARs was to restrict the flow of sensitive information, not delay and restrict sales of non-sensitive technology.

For decades we've kept Iran's F-14s grounded through restricting their acquisition of parts and technical data. Recently we've allowed surplus F-14 parts out on the free market, guess what? Another one: We fast tracked getting India U.S. civil nuclear technologies in an unheard of 18 months. The government can't buy toilet paper in 18 months. Here's one I have pinned up on my bulletin board from last fall. NASA Administrator Michael Griffin during a luncheon address of the Society of Experimental Test Pilots, informed the membership that any thoughts that taxpayer funds used by NASA to develop new technology would be to the benefit of U.S. industry was absolutely wrong. Our government doesn't want to be accused of subsidizing U.S. business. Let me add another Huhhh….?

Governments and business opportunists have been tripping over each other to inject all the latest technologies into China. We've managed to completely see only what we want to see with respect to China's ambitions and goals. Our "hopes" are that as China travels down its future path that it will be so intertwined with all the other nations of the world that it will see the light and live peacefully in the world community. Through greed and ambition we've provided China with the impression that it holds all the cards and it is not at a loss to take full advantage of that.

I know I don't have answers to any of the complicated issues that confound our government. Patents, copyrights, security and even ITARs are just a joke to many countries and organizations throughout the world. So we need to find better ways to keep our technological innovations secure; technology creation is what we do best. Along with our creative and entrepreneurial spirit, the U.S. has the proper environment to develop and nurture new technologies. We need to start treating technologies we develop as national treasures to prudently share with the rest of the world. We shouldn't just give them away, particularly in those instances where there's potential for them to be used against us.

ITARs may be an effort to limit the unrestricted propagation of sensitive technology relating to military programs, while bureaucracy and political agendas may offer "workarounds" for the bigger players. As with all regulations, ITARs need review and updating over time and as circumstances and the way the world works change. Otherwise those regulations can become ineffective or unmanageable. Sensitive technology transfer is not just a military issue. It's an important matter for all leading-edge technologies from semiconductor manufacturing to nuclear weapons. Security of our leading-edge technology is one plate the government has to keep spinning. It can't be allowed to fall. ▮▮

Pete Yeatman, Publisher
COTS Journal

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The Inside Track

DRS Technologies Awarded Contract for Kiowa Sighting Gear

The U.S. Army Aviation and Missile Command (AMCOM) at Redstone Arsenal in Huntsville, AL has awarded a $51 million contract to DRS Technologies to support the manufacturing of Mast Mounted Sights (MMS) installed on OH-58 Kiowa Warrior attack helicopters. For this order, DRS will provide depot repair, spares and field service support for the MMS, as well as post-production, engineering and depot support for obsolescence mitigation and engineering change proposals. The work for this award will be accomplished by the company's DRS Sensors & Targeting Systems – Optronics Division in Melbourne and Palm Bay, Florida. Product deliveries and services are expected to continue through 2008.

The MMS contains a suite of sensors, including a high-resolution television camera for long-range, low-light target detection and an upgraded thermal imaging sensor supporting navigation, target acquisition and designation. A laser rangefinder/designator in the unit provides precise target location and guidance of Hellfire missiles and Copperhead artillery rounds, while a boresight assembly provides in-flight sensor alignment.

Installed above the rotors of the helicopter, the MMS incorporates sighting system technologies that are crucial to the missions and survivability of U.S. ground forces. It provides the helicopter with improved target acquisition performance, greater stand-off ranges and reconnaissance capabilities. The MMS enables the Kiowa to fight during both day and night from the maximum range of its weapons systems with minimum exposure to enemy threats.

DRS Technologies
Parsippany, NJ.
(973) 898-1500.
[www.drs.com].

Figure 1

The Mast Mounted Sights (MMS) installed on OH-58 Kiowa Warrior attack helicopters contain a suite of sensors, including a high-resolution television camera for long-range, low-light target detection and an upgraded thermal imaging sensor. Shown here is an OH-58 Kiowa helicopter at the Forward Ammunition and Reaming Point at Contingency Operating Base Speicher in Iraq.

ACC Gets $8 Million Added to Navy Anti-Sub Warfare Contract

The U.S. Navy has award $8.1 million to Advanced Acoustic Concepts (AAC) for a modification to a previously awarded Naval Sea Systems Command (NAVSEA) contract. The NAVSEA funding will be used for the conversion/installation of seven AN/SQQ-89(V) Scaled Improved Performance Sonar (SIPS) kits and engineering services in support of Anti-Submarine Warfare (ASW) improvements across multiple surface ship platforms and programs.

The SIPS kits will be installed on DDG and CG platforms to enhance active and passive submarine and torpedo detection, classification and localization capabilities. SIPS provides an affordable solution to modernizing legacy surface ASW platforms using an accelerated and mission-configurable approach developed by a team of small businesses, university laboratories and the U.S Navy, for which AAC serves as the prime integrator.

According to ACC, the deal is in keeping with the Navy's vision of commonality across multiple platforms. The goal is for advanced technologies that will be paid for once, but used many times. For example, the LCS ASW Mission Package is leveraging technology introduced by SIPS, facilitating interoperability of deployed mission package sensors.

Advanced Acoustic Concepts
Hauppauge , NY.
(631) 273-5700.
[www.aactech.com].

Future Combat Systems Completes Eight-Month Experiment

Boeing and Science Applications International Corp. (SAIC), the Lead Systems Integrators for the U.S. Army's Future Combat Systems (FCS) program have announced the successful completion of an eight-month field experiment said to be the cornerstone of soldier evaluation activities and an important step toward the early infusion of key FCS capabilities to the current force. Experiment 1.1, spanning July 2006 through February 2007, is a three-phase effort that combines laboratory, field and demonstration activities with soldier testing of early FCS prototypes.

The experiment was designed to help reduce program risk and provide early feedback into the development, integration and verification process of the program. It also helped to enable the early spin out of key capabilities to the current force in 2008. In one phase of the experiment, the FCS team, which included more than a dozen U.S. Army soldiers as observers, demonstrated Non-Line-of-Sight (Figure 2) Launch System networking, Distributed Fusion Management capabilities, Unattended Ground Sensors capabilities, Joint Tactical Radio System Ground Mobile Radio performance, and interoper-

Figure 2
Part of the FCS Experiment 1.1 was the demonstration of the Non-Line-of-Sight Launch System networking. Among the combat vehicles in the FCS program is the Non-Line-of-Sight-Cannon (NLOS-C), which will serve as the key indirect fire support system for FCS.

ability with current Army and Marine Corps systems.

The final demonstration phase of Experiment 1.1, which was conducted January 2007 to February 2007 at the White Sands Missile Range and Ft. Bliss test complex, included 36 soldier participants who provided "hands-on" feedback of early FCS prototypes, while exercising initial doctrinal concepts for employing these new capabilities. Phase 3 represented the first time soldiers collectively employed FCS systems in a live training environment and used an FCS computer-based training support package.

Boeing Integrated Defense Systems
St. Louis, MO.
(314) 232-0232.
[www.boeing.com].

SAIC
San Diego, CA.
(800) 430-7629.
[www.saic.com].

Navy Buys Two More Fire Scout UAVs from Northrop Grumman

The U.S. Navy has awarded Northrop Grumman Corporation $16 million for two more MQ-8B Fire Scout (Figure 3) Vertical takeoff and landing Tactical Unmanned Air Vehicles (VTUAV) and to assist the Navy in refining the Fire Scout concept of operations. Including this award, the Navy has a total of nine Fire Scouts on contract with Northrop Grumman. The two air vehicles will help the Navy to complete operational test and evaluation as well as some spiral development preparations and test of future payloads.

System design work on the Fire Scout is performed at the Unmanned Systems Development Center in San Diego. The Fire Scout is assembled at the Unmanned Systems Center in Moss Point, MS. Fire Scout is based on a commercial-off-the-shelf Schweizer 333 manned helicopter manufactured in Horseheads, NY. The baseline design has proven a highly reliable and effective platform with extensive operating history.

The MQ-8B successfully completed the first series of autonomous flight testing the third week of December at Naval Air Station Patuxent River. The next two years of planned activity on this program include entering low-rate initial production, operational evaluation on a Littoral Combat Ship and operational capability in 2008. The embedded computers and the payload interface unit aboard the MQ-8B are 3U CompactPCI form-factor boards.

Northrop Grumman Integrated Systems
El Segundo, CA.
(310) 332-1000.
[www.is.northropgrumman.com].

Figure 3
The MQ-8B Fire Scout is a vertical takeoff and landing tactical UAV (VTUAV). The embedded computers and the payload interface unit aboard the MQ-8B are 3U CompactPCI form-factor boards.

General Dynamics Awarded DARPA Contract for Next-Gen Wireless Nets

The Defense Advanced Research Project Agency (DARPA) has awarded General Dynamics C4 Systems one of three research and development contracts for the Wireless Adaptable Network Node (WANN). General Dynamics will lead a team in the development of a new, software-based, portable radio that will enable future networked communications in urban areas or across a widely distributed battlespace for U.S. military forces. The phase-one contract is valued at $1.4 million. The Air Force Research Laboratory is the contracting agency for DARPA's Strategic Technology Office.

The WANN program will combine wireless communication and networking technologies along with commercial-off-the-shelf products to develop a low-cost radio-node that will enable the military's next generation of intelligent, rapidly deployable, distributed communication networks. WANN is part of DARPA's "Wireless Network after Next" program to provide military forces with reliable and highly available battlefield communications at a low system cost. The WANN program consists of four phases. General Dynamics will deliver the phase-one radio design to DARPA by June 2007. The contract includes an option for phase-two development and testing following a down-select decision expected third quarter 2007. Phases three and four will be awarded at a later date.

General Dynamics C4 Systems
Scottsdale, AZ.
(877) 449-0600.
[www.gdc4s.com].

Panasonic Rugged Laptops Selected for Marine Corp Network

As part of EDS' management of the Navy Marine Corps Intranet (NMCI), the Information Technology backbone of the Department of the Navy (DoN), Panasonic Computer Solutions has been selected to provide rugged notebook computers (Figure 4) to military users of the NMCI. NMCI provides the DoN with a full range of network-based information services on a single, enterprise-wide intranet. With Panasonic as part of the alliance, approximately 72,000 NMCI users—from warfighters to civilians—will have access to rugged computers designed to be reliable in mission-critical environments.

Figure 4
The Panasonic Toughbook computers are ruggedized with cases constructed of magnesium alloy and include shock-mounted and removable hard drives. With battery life of approximately 6 hours, these units are certified to the MIL-STD-810F, tested to withstand drops, shocks, vibration and extremes in temperature.

The Panasonic Toughbooks provided under this contract are ruggedized with cases constructed of magnesium alloy and include shock-mounted and removable hard drives. With battery life of approximately 6 hours, these units are certified to the MIL-STD-810F, tested to withstand drops, shocks, vibration and extremes in temperature. Among the industry's most secure, these Toughbooks come equipped with cable lock slot, the Trusted Platform Module (TPM v1.2) security chip, BIOS-level support for Absolute's Computrace anti-theft application, as well as optional fingerprint scanners. In addition, users have the option of multiple wireless options—WLAN, WWAN, GPS and Bluetooth.

Panasonic Computer Solutions
Secaucus, NJ.
(800) 662-3537.
[www.panasonic.com/toughbook].

COTS Websites

www.dsp.dla.mil

Defense Standardization Program Site Provides a Unique Gateway

The Defense Standardization Program Office holds the responsibility to champion standardization throughout the DoD to reduce costs and improve operational effectiveness. Its job is to identify, influence, develop, manage and provide access to standardization processes, products and services for warfighters, the acquisition community and the logistics community to promote interoperability, reduce total ownership costs and sustain readiness. The program is intended as a comprehensive, integrated standardization effort linking DoD acquisition, operational, sustainment and related military and civil communities.

The Defense Standardization Program's Web site is both a resource for standards information and documentation and a gateway to all the myriad standardization bodies—both government and commercial—that are relevant to the military. Sections of the Web site include resources on Interoperability with links to some key DoD programs to promote interoperability; a page for locating and downloading online specifications and standards; a library of policy memos, case studies, key resources and more; direction on the use of Non-Government Standards (NGS) and cooperation with NGS bodies; information on Joint Standardization Boards; and information on standards courses and Defense Standardization Program conferences.

Defense Standardization Program Office, Fort Belvoir, VA. (703) 767-6888. [www.dsp.dla.mil].

Special Feature

PC/104 in the Military

PC/104 and EPIC Advance into Serial Territory

PC/104 and EPIC have become entrenched as solutions for rugged, small form-factor military applications. Now PCI Express and USB are spicing up their functionality.

Jeff Child
Editor-in-Chief

PC/104—and its wider community of form-factors including PC/104-Plus, PCI-104, EPIC and EPIC Express—occupies a unique niche in embedded applications—such as aboard aircraft and inside missiles—where backplanes won't fit or are otherwise impractical. PC/104 has won designs in a wide range of new and retrofit embedded computing devices used across all branches of the U.S. armed forces.

Military engineers select PC/104 technology because of the ruggedness inherent in its stacking architecture. This stacked multi-board system provides for a shock- and vibration-resistant off-the-shelf computing solution by eliminating backplanes and metal card cages, making PC/104 ideal for military vehicles such as tanks or even Humvees (Figure 1). Finally, the light weight of PC/104 systems make PC/104 an ideal architecture for portable systems carried by soldiers, such as military radios.

Dynamic changes aren't part of PC/104's character, but the last couple years or so there's been some dramatic advances that have bolstered PC/104 and the community of vendors surrounding it. Perhaps the most significant news to spring from the PC/104 community was the roll out a couple years ago of the Embedded Platform for Industrial Computing or EPIC form-factor.

While not an official creation by the PC/104 Consortium, the EPIC spec was developed jointly by a cross section of major PC/104 players, including Ampro Computing, Micro/Sys, Octagon Systems, VersaLogic and WinSystems. The EPIC form-factor fills the need for a mid-range-sized form-factor between that of PC/104 and the EBX motherboard standard. Later, the PC/104 Consortium announced its adoption and management of the EPIC standard.

A recent EPIC product example is Kontron's EPIC/PM (Figure 2). Based on the Pentium M 745 processor, the board offers complete PC/104-Plus functionality with both PCI and ISA expansion. For cost-sensitive applications or fanless operation, the Kontron EPIC/PM is also available in ULV Celeron M 373 with 1 GHz (512 KB L2) or Intel processor Celeron 800 MHz (0KB L2) versions.

Meanwhile, PCI Express has moved into the desktop space, but not directly into the PC/104 form-factor. Instead, PCI Express has been married to PC/104's larger and younger cousin, the EPIC form-factor. The same group of five embedded SBC manufacturers that created the EPIC form-factor announced the publication of the EPIC Express Specification, which adds high-bandwidth PCI Express I/O expansion to EPIC form-factor SBCs without sacrificing support for legacy PC I/O.

Figure 1

The inherent ruggedness of PC/104 comes from its stacking architecture. This stacked multi-board systems provides for a shock- and vibration-resistant off-the-shelf computing solution by eliminating backplanes and metal card cages, making PC/104 ideal for military vehicles such as tanks or Humvees.

The specification defines the EPIC SBC interface as well as the mechanical layout, connectors and pin definitions for EPIC Express I/O Expansion cards. The PCI Express interface itself consists of a high-performance connector and design rules to support up to four EPIC Express I/O expansion cards with up to six total PCI Express devices in a unique stacking configuration. The specification accomplishes this without terminating support for legacy PC devices and buses that are used pervasively in embedded applications.

Stackable USB Comes on the Scene

The DoD gave the thumbs up years ago for USB to be used in military programs, but it has been slow to reach its potential in the general embedded realm, much less the military market. Micro/sys last month helped smooth the way with the release of the StackableUSB Specification. It defines a standard for stacking I/O boards onto a single board computer using the popular USB 2.0 interface.

A single board computer, operating as a host, can communicate to multiple USB peripheral cards directly through mating USB 2.0 connectors resident on the CPU and I/O cards. This format eliminates cables, reduces pin count, and requires a smaller connector footprint than traditional interconnect architectures. By securely bolting together to increase reliability and mobility in rugged or harsh environments, the StackableUSB format features a USB point-to-point architecture where connections are routed up a stack to the next peripheral in the stack.

Each StackableUSB connector supports up to eight USB peripheral devices in the stack without a hub. There are several features USB I/O supports that have not been available in the past when using traditional stacking architectures such as PC/104 and PC/104-Plus. USB supports automatic enumeration that allows the host to detect devices plugged into the stack and to install the drivers necessary for the system to operate with minimal human intervention. USB also supports power management so that USB peripherals or devices can be placed in a low power mode to conserve power, an issue that is paramount in embedded systems relying on battery-backed power or environments where heat generation is of key concern. USB 2.0 also offers increased data bandwidth to support today's high-speed A/D, and DAC data rates.

Implementation of USB on a single board computer or I/O card is easy and cost-effective. Inclusion of USB in most popular chipsets and many microcontrollers makes this an easy and inexpensive implementation compared to PCI and PCI Express I/O. USB also offers a range of speeds, from 480 Mbits/s at high speed, 12 Mbits/s at full speed and 1.5 Mbits/s at low speed. This provides embedded system designers a road map into the future for increasing their system throughput as technology advances.

Micro/sys hopes the StackableUSB spec will open up a market for USB I/O to move into embedded OEM applications. Typically such systems have not tolerated USB devices well because of constricted spaces, high vibration, or special packaging or enclosure requirements. The spec is available at www.stackableusb.org and is published by Micro/sys.

Micro/sys has also released the first StackableUSB CPU board on a Pentium III processor. In addition to all standard PC features, the SBC1685 (Figure 3) also includes a Gigabit Ethernet port, four USB 2.0 high-speed ports, four USB 1.1 full-speed ports and a CompactFlash interface. SBC1685 also offers a printer port, keyboard, mouse, external IDE and floppy controllers, and a watchdog timer. With up to 256 Mbytes of socketed SDRAM, and full PC-compatibility, high-performance embedded control systems can be implemented on this small industrial form-factor (PC/104-size) SBC.

Specialty Enclosure Designs

An ever-growing number of airborne, marine, handheld and vehicular applications make use of PC/104's modular, off-the-shelf architecture. Many of those applications require a certain degree of sophistication when it comes to electronics enclosures and packaging. That's particularly the case for applications with demanding environmental specifications where the system is tasked to operate reliably in harsh field conditions. Certainly the lack of a backplane and the use of a pin-and-socket mating connector naturally help make PC/104 inherently rugged. That said, dealing with heavy loads of shock and vibration energies, submergence in seawater, extreme temperature operation or electromagnetic pulses (EMP) make a sound mechanical design for PC/104 systems all the more critical.

Crafted especially for military program requirements, a growing assortment of standardized PC/104 enclosure and chassis solutions is available from several PC/104 vendor companies. These enable system developers to fast track the development of ruggedized systems while minimizing the use of costly Mil-Spec or custom parts.

Figure 2

A recent EPIC product example is Kontron's EPIC/PM. Based on the Pentium M 745 processor, the board offers complete PC/104-Plus functionality with both PCI and ISA expansion.

In some cases, the PC/104 vendor takes such a system designed for a specific program and makes it available for general use. An example is Parvus' External Bus Monitoring (EBM) device for the Communication Navigation and Identification (CNI) system of the F/A-22. This device provides general-purpose data-logging functionality over a MIL-STD-1553 databus. It is capable of reading up to four CNI asynchronous buses and transmitting on two additional channels.

Mounted within a Parvus EBX Quarter-Turn Dzus Rail Enclosure that meets military mounting specification MS25212, the PC/104-based unit incorporates an x86 CPU, high-efficiency power supply, dual 1553 bus interface, embedded audio card and dual PC/104 stack motherboard, supplying various services to the CNI system, including MIL-STD-1553 compatibility, 8-character LED display, keypad, audio, ATA drives and thermal measurement sensor.

The EBM's front panel has several controls, including two switches (for power and program status) and a four-position keypad. Two PC Card sockets are positioned behind a hinged access door on the front panel to enable the use of removable ATA flash mass storage. A user access panel on top of the chassis provides access to the internal PC peripherals, such as keyboard, video, mouse, COM1 serial, reset and speaker. The rear panel includes three size-12 circular MIL-C-38999 connections.

Heat Issues Plague Stacked Systems

Thermal management in a board—and, indeed, in a system—becomes a critical reliability concern with the latest crop of hot-running GHz+ microprocessors, for example. And it can be difficult to handle the heat rising from a PC/104 CPU board through a stack of I/O boards and to safely dissipate the heat and keep the system cool. At the very least, extra space for ventilation or fan clearance may be necessary, adversely impacting space efficiency.

The thermal management issue is of particular concern to military designers, who resist using fans and must often make do with only conduction cooling. Heat management in tightly sealed systems is of ultimate concern. If a fast microprocessor resumes activity after sleep mode, for example, it creates a huge surge of heat going up through the stack. If the board above it is, say, an analog data acquisition board, the rising temperature will affect its calibration and adversely impact the validity of its measurements.

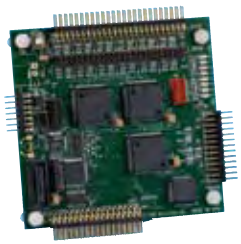

Figure 3

Micro/sys' first Stackable USB CPU board is based on a Pentium III processor. In addition to all standard PC features, the SBC1685 includes a Gigabit Ethernet port, four USB 2.0 high-speed ports, four USB 1.1 full-speed ports, and a CompactFlash interface. SBC1685 also offers a printer port, keyboard, mouse, external IDE and floppy controllers, and a watchdog timer.

In theory, a heat transfer mechanism such as a machined aluminum arm could be run up through a PC/104 stack to route the heat away from a hot CPU. Not only is this an awkward solution, but it could also have disastrous effects. At certain vibration frequencies, for example, the vibration dynamics between the rigid arm and non-rigid board stack may eventually cause the arm to break loose.

EPIC Beats the Heat

With EPIC, in contrast, the CPU is located out in the open where it's much easier to cool and where I/O expansion boards do not have to endure its rising heat. Moreover, the added real estate of EPIC allows mounting holes to be placed on the sides of a CPU to accommodate a cooling arm and create a wholly rigid heat-transfer mechanism that can handle every vibration range that's of interest to military designers.

Beyond the heat issue, PC/104 also has a drawback for systems with heavy input/output requirements, trading off either space efficiency or reliability. The PC/104 specification requires 0.5-inch keep-out areas beyond the edge of a board to accommodate the overhang of right-angle connectors. The effect of this is to increase the real estate required for a board about 44 percent—from 13.5 square inches up

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Figure 4

The XE-900 from Octagon Systems incorporates the 32-bit, low-power VIA Eden CPU family with three versions available: 400 MHz, 733 MHz and 1 GHz. It integrates video, serial ports, Ethernet, digital I/O, USB and PC/104 and PC/104-Plus into a single card. The board's conduction-cooling system eliminates the need for a fan even at 1 GHz.

to 19.5 square inches. Moreover, a 0.5-inch connector removal area must also be taken into account, bringing the total area required for using a 13.5-square inch PC/104 board to 26.5 square inches.

An example EPIC product tailored for harsh environment military applications is the XE-900 from Octagon Systems, which includes a rich family of I/O functions. The XE-900 incorporates the 32-bit, low-power VIA Eden CPU family with three versions available: 400 MHz, 733 MHz and 1 GHz. It integrates video, serial ports, Ethernet, digital I/O, USB and PC/104 and PC/104-Plus into a single card. The XE-900 was designed to operate in extreme environments and those where reliability is a major concern. It will withstand high shock and vibration, and operates in a -40° to +85°C temperature range.

The XE-900 features two USB ports; six RS-232/422/485 serial ports; 24 lines of bit-programmable, digital I/O with 16 mA sink/source capability; 10/100 Base-T Ethernet, CRT and flat panel video, PC/104 and PC/104-Plus expansion and a conductive-cooling system (Figure 4). The conduction-cooling system eliminates the need for a fan even at 1 GHz.

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Tech Recon

Switched Fabrics

Bandwidth and Cost Drive ATCA/MicroTCA Fabric Choice

Increasing bandwidth demands are bringing ATCA and MicroTCA into military developers' mindshare. Choosing a switch fabric flavor for those platforms calls for careful consideration.

Sivaprasad Raghavareddy,
Technical Marketing MicroTCA, Embedded Communications Computing, Motorola

The demand for higher speed and more bandwidth seems unstoppable. The ongoing convergence of computing and communications fits perfectly into the U.S. Military's goals of migrating to a network-centric operational paradigm. This trend is apparent not only among defense, aerospace and federal organizations, but in medical and scientific markets as well. Existing architectures are feeling the strain.

Like their civilian market counterparts, military end users are also demanding higher quality of service (QoS), requiring the increased use of high-availability systems. These are some of the factors that are driving the adoption of new interconnect technologies in embedded systems. The issues of performance, cost, modularity, reuse, distributed processing and system-wide interconnects only further complicate the decision of which technology is appropriate.

Switched fabric interconnects provide point-to-point connection between two devices, regardless of how many devices are connected to the fabric. The PICMG 3.x specifications for AdvancedTCA (ATCA) can accommodate a range of switched fabric technologies in the system's backplane, including Ethernet, PCI Express, InfiniBand and StarFabric.

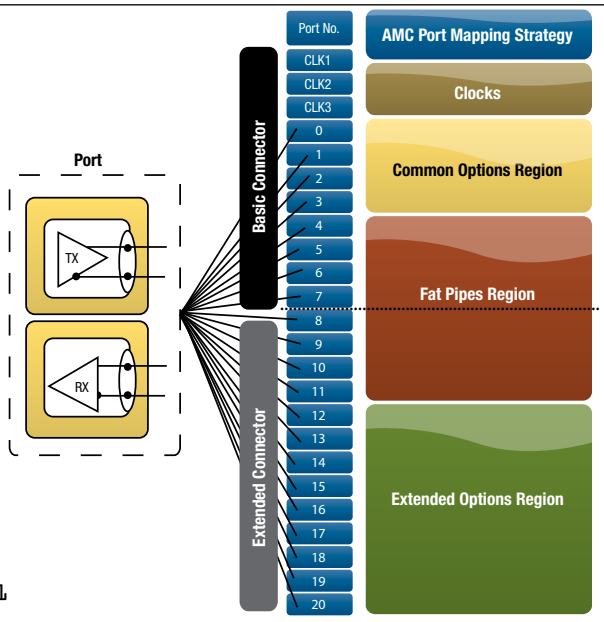

Figure 1

Broken out here are three primary regions defined for AMC port mapping. A common options region is defined to support basic and essential interfaces. The fat pipe region is defined to support large data path connections. An extended options region is loosely defined as an extension of fat pipes or common options region to support additional bandwidth requirements.

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Small-Footprint MicroTCA

Advanced Mezzanine Cards (AMCs) are hot-swappable modules originally designed to be used as plug-in modules in an ATCA system. MicroTCA is a new standards-based system constructed by allowing AMC modules to be plugged into a system backplane, and provides a small system footprint, low power and low cost with advanced management capabilities.

The AMC.0 base specification provides a physical framework for the fabric interface, while the AMC.x subsidiary specifications define how to overlay a specific switching interconnect technology onto the AMC.0 fabric interface physical framework. The AMC specification provides a total of 21 ports that are optimized for current and emerging LVDS (Low Voltage Differential Signaling) interconnect standards, such as PCI Express (AMC.1), Gbit Ethernet (AMC.2), SATA/SAS (AMC.3) and Serial RapidIO (AMC.4).

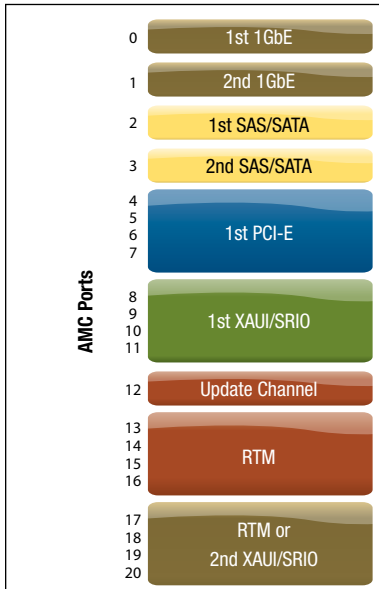

Figure 2

Shown here is one possible AMC port mapping that can satisfy the applications requiring low latency at high transmission rates, such as those in military and aerospace. Port 0 and 1 are for Gbit Ethernet for redundant control plane communication; Ports 2 and 3 are assigned to storage; Ports 4 to 7 are used for PCI Express to communicate with IO devices; and ports 8 to 11 and ports 17 to 20 are for x4 Serial RapidIO or for 10 Gbit interface for time-critical communications.

As shown in Figure 1, three primary regions are defined for port mapping. First is a common options region that is defined to support basic and essential interfaces. Second is a fat pipe region that is defined to support large data path connections. And third is an extended options region that is loosely defined as an extension of fat pipes or common options region to support additional bandwidth requirements.

As with the ATCA specifications, system designers have the flexibility with AMC to choose the appropriate AMC.x subsidiary standards based on their specific needs in maximizing the overall system efficiency of the proposed end ap-

plication. For example, Figure 2 provides one possible port mapping that can satisfy the applications requiring low latency at high transmission rates, such as those in military and aerospace.

Comparing Performance

The efficiency of Serial RapidIO is higher for small data packet sizes, while Gbit Ethernet is lower when used with the TCP protocol. As the protocol data unit size increases, PCI Express increases in efficiency compared to the other protocols. This is primarily because Serial RapidIO has a limit of 256 bytes on the payload data with each packet sent.

The respective packet sizes of Serial RapidIO and PCI Express technologies reflect their primary application focus. Serial RapidIO reaches its highest efficiency at a packet size of 256 bytes, which is also the maximum, and stays flat from there on. Serial RapidIO supports 256 traffic classes, intended to optimize capacity for streamed data alongside burst data, and accounting for substantial future extensibility; for example, processing of video applications. PCI Express reaches optimal efficiency at larger packet sizes, which makes it suitable for applications where a peripheral needs to transfer large amounts of data from the host or another device, such as remote data sensing and transfer at military locations.

PCI Express also offers backward compatibility with legacy PCI software. The primary weakness of PCI Express is evident in its dependence on a single-host, multiple-peripheral communication mode. This characteristic mandates multiple root complexes to support multiple hosts at the same time or a non-transparent bridge resulting in multiple segments.

On the other hand, Serial RapidIO supports multiple hosts by default with cache coherency. This enables users to take advantage of Serial RapidIO by implementing multiprocessing distributed systems. In a multi-host system connected directly to a single Serial RapidIO switch, network saturates at 95 percent of link utilization due to the control symbols that take up some link bandwidth. However, for a multi-stage network, link utilization may go as low as 33 percent depending on the configuration.

Gbit Ethernet has a lower protocol efficiency compared with PCI Express and Serial RapidIO. Furthermore, using UDP is more efficient than TCP due to its connectionless nature versus TCP's connection-oriented nature. Terminating TCP/IP demands significant additional processor overhead. The designer is faced with either using a TCP Offload Engineer (TOE) or accepting reduced application performance and/or features.

That said, Gbit Ethernet provides seamless connectivity beyond the backplane to the outside world. These technology advantages, combined with the commercial benefits, make Gbit Ethernet the ideal technology for control plane communications. Meanwhile, PCI Ex-

press or Serial RapidIO may be appropriate for data plane communication. With increasing availability of 10 Gbit Ethernet solutions, users should even be able to use Ethernet for data plane communication, provided that the payload data per packet is relatively higher.

Going Beyond Telecom

The traditional configuration of MicroTCA today is as shown in Figure 4a, a MicroTCA chassis designed for central office telecom applications. Figure 4b shows how standards-based platforms can be extended into access and edge networks, whether that be in an enterprise-like command base or in-theater in a desert environment on a mobile communications platform. This ruggedized MicroTCA packaging shows how external environments—with temperature and humidity concerns—, and vehicle-mounted environments—with shock and vibration concerns—can be accommodated. Applications include mobile military networking node stations and deployed access points. For example, a ruggedized MicroTCA system that provides WiMAX connectivity can be placed on a military truck to provide connectivity among moving entities.

Hot-swap functionality supported by the various AMC.x interconnects means it is possible to create highly available systems using MicroTCA or ATCA. PCI Express provides Reliability, Availability

Figure 3a

Figure 3b

The traditional configuration (a) of MicroTCA today is appropriate for benign military environments. A ruggedized MicroTCA packaging (b) can be used in applications like a mobile military networking node station or deployed access point. For example, a ruggedized MicroTCA system that provides WiMAX connectivity can be placed on a military truck to provide connectivity among moving entities.

and Serviceability (RAS), which consists of three fundamental components: A reliable protocol architecture; device-level protocol error detection, correction and reporting; and device-level requirements for support of a hot-plug usage model based on current industry standards.

This makes PCI Express appropriate for applications that require RAS from components, all the way up to system level. With End-to-end Cyclic Redundancy Check (ECRC) and Link Cyclic Redundancy Check (LCRC), PCI Express provides a reliable data transfer from source to destination. Serial RapidIO provides RAS at the hardware level and traffic management features as well.

Creating a Mainstream Market

Switched interconnects supported by MicroTCA enable high availability and better bandwidth. This makes it usable in a wide range of target market segments, such as the defense, telecom and medical industries. The ATCA and MicroTCA specifications provide a range of connectivity options. This flexibility is both a blessing and a curse. If vendors and users adopt multiple fabric technologies, the market will effectively fragment into multiple smaller ecosystems. This increases the risk that these open standards-based technologies will not fulfill their market potential due to their inability to realize economies of scale.

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Tech Recon

Switched Fabrics

Point-to-Point Serial Interconnects
Edge Out Switched Schemes

High-speed serial interconnect schemes are vital in a lot of high-bandwidth military applications. While switched fabrics get a lot attention, simpler point-to-point interconnect schemes are a better choice for some situations.

Dave Barker, Vice President Market Development
VMETRO

High-speed serial interconnect (HSSI) technology can fill several roles in military embedded systems: chip-to-chip, board-to-mezzanine, board-to-board and sensor-to-subsystem interconnects to name a few. Use of HSSIs simplifies cabling, improves bandwidth and enhances system architecture by allowing more flexible interconnects than parallel buses. Military applications with a large appetite for fast interconnect links range from radar processing to SIGINT to integrated missile defense systems.

An example along those lines, is Lockheed Martin's instrumentation and testing work the company is doing for the Aegis Ballistic Missile Defense (Aegis BMD) Weapon System (Figure 1). For data recording in the system, Lockheed uses a VME platform that does playback of the recorded data over 10 Gbit Ethernet. The Aegis BMD Signal Processor (BSP) is now in development and will be installed in Aegis BMD ships beginning in 2010. The Aegis BMD Weapon System seamlessly integrates the SPY-1 radar, the MK 41 Vertical Launching System, the SM-3 missile and the weapon system's command and control system.

Many HSSI Choices

With so many high-speed interconnect options available these days, it's hard to put a precise definition on high-speed serial interconnects. As the name implies these are high speed, but there is no clear-cut definition of what the speed of high speed is. Based on today's technology, speeds start at 1 Gbit/s and move up from there. Currently the highest achievable speed in off-the-shelf silicon is about 10 Gbits/s, but the upper limit keeps increasing over time.

As the term HSSI also implies, these technologies communicate over serial links; namely, Low Voltage Differential Signaling (LVDS) over differential pairs, with one pair for transmit and one pair for receive—a total of 4 wires for a full duplex connection. Data is encoded using a method called 8b/10b encoding. Another common characteristic of HSSI technology is that the 8b/10b encoding/decoding and the SerDes are implemented in hardware in the chips that provide HSSI links. Aurora, Serial FPDP, Serial RapidIO, PCI Express and Gigabit Ethernet are protocols that are all built on top of high-speed serial interconnect technologies.

Two basic protocol types of HSSIs exist: point-to-point and switched fabric. Much of the recent discussion has been around advantages and usage of various popular switched fabrics, but in many

Figure 1

The Aegis Ballistic Missile Defense (Aegis BMD) Weapon System is an example of a system with a large appetite for high-speed data movement. For data recording in the system, Lockheed uses a VME platform that does playback of the recorded data over 10 Gbit Ethernet. The Aegis BMD Weapon System integrates the SPY-1 radar, the MK 41 Vertical Launching System, the SM-3 missile and the weapon system's command and control system.

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defense DSP applications point-to-point protocols are a better fit.

Point-to-Point Fits the Problem

Point-to-point HSSIs solve the types of problems many defense DSP systems present. In a defense system, data typically streams from a sensor, through a pre-processing system, into a general processing system, and usually to some type of operator display or possibly into a mass storage device such as a high-speed data recorder. A simplified view of such a system is shown in Figure 2.

In any system design, data paths are well-known from the inception of the architecture, and are fixed—they don't change during system operation. The streaming nature of these systems calls for an efficient, fast and lightweight point-to-point protocol. Point-to-point HSSI technology has several distinct advantages over alternative approaches. First, the complexity of parallel interconnects is eliminated, with no large bulky connectors and cables or backplanes. Second, issues such as data skew and signal quality under loading associated with parallel buses are eliminated. And finally, overall throughput is increased, for two reasons. First, there is no waiting for parallel bus arbitration. Second, serial links are faster and full-duplex. A new generation of SerDes devices is now capable of delivering 10 Gbits/s in a serial lane of an HSSI.

Meanwhile, point-to-point topologies have different advantages over switched serial fabric topologies. With point-to-point connections, addressing information isn't required; therefore packets carry less packet overhead and more data. By not requiring switching elements, point-to-point protocols not only are simpler to design with and implement, but are faster and have lower latency than switched topologies. There is no waiting for switch arbitration or overhead—when the data transfer is ready, it can begin unimpeded.

Basics of Point-to-Point

In a very simple form, a full-duplex point-to-point HSSI can be implemented on two LVDS differential pairs. Consider for example such a two-pair scheme where the clock is encoded on the data signal. Data is encoded using a 8b/10b scheme, meaning a balanced number of 1s and 0s representing each byte of data, and a total of 10 bits transferred for each byte. It's that balance that allows the speed to be cranked up—the DC voltage level of the resulting encoded signal averages midway between the two signal levels, helping with clock recovery and noise immunity. On a 2.5 Gbit/s link, 250 Mbyte/s throughput can be achieved using this encoding—and more on faster links such as 10 Gbits/s.

For more throughput, full-duplex point-to-point lanes can be bonded together, perhaps 4x wide, or even up to 32x wide, with data striped across lanes. The complexity of the link increases but the point-to-point protocols can be scaled to meet the needs of the application. The most common bonded widths are 4x and 8x. These point-to-point schemes can be

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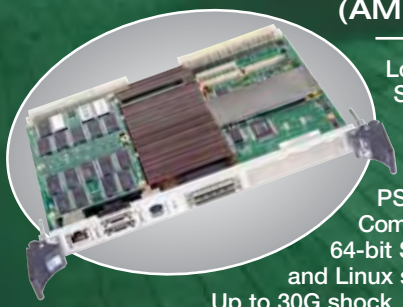

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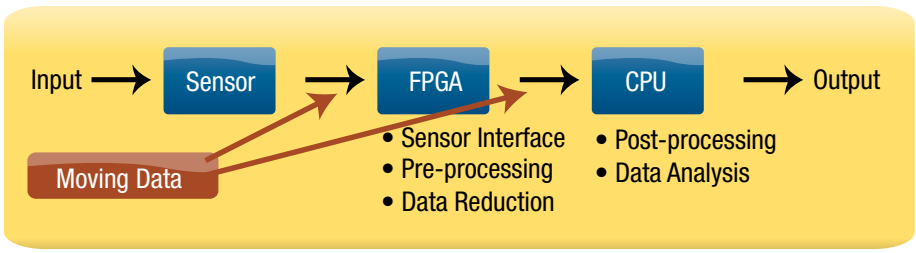

Figure 2

Shown here is a simplified view of a defense DSP system. Data streams from a sensor, through a pre-processing system, into a general-processing system and usually to some type of operator display or possibly into a mass storage device such as a high-speed data recorder.

implemented in fixed silicon, but more and more often designers are opting to implement in FPGAs. This gives them the opportunity to combine data links with data processing in ways tailored to meet the problem at hand.

Point-to-Point Protocols

One protocol getting attention as a point-to-point solution is Aurora. Designed specifically to implement simple point-to-point interconnects, Aurora is a scalable, lightweight link-layer protocol. Xilinx created the Aurora specifications to enhance the design utility of their FPGAs, but has opened the specification up so any designer can work with them in any FPGA family using the supplied free IP. It provides a transparent interface to the physical serial links, allowing upper layers of proprietary or industry-standard protocols, such as Ethernet and TCP/IP, to easily use these high-speed serial links. This leads to higher connectivity performance while preserving software infrastructure investment.

While Aurora doesn't define error detection or recovery mechanisms, or a data switching/addressing scheme, it does do one thing well—move data quickly, with limited overhead. Its speed is limited only by the SerDes used, and lanes can be bonded together to provide more bandwidth on a single logical link.

A slightly more sophisticated protocol in this space is Serial FPDP, based on the ANSI/VITA 17.1 standard. A serialized version of the Front Panel Data Port specification, Serial FPDP is simple, easy to use and popular with designers of sensors and data acquisition hardware. It supports up to 2.5 Gbit/s links, and works over copper or fiber interfaces. It also includes optional features such as data copying, data loopback and flow control. The VITA Standards Organization is looking at higher data rates and lane bonding to help increase throughput further.

Three Application Examples

To help illustrate some of the advantages of point-to-point HSSIs in defense systems, consider three application examples. The first concentrates on combining data streams from a distance. The second involves very high-speed data recording. And the third uses FPGAs to craft a highly integrated solution.

In the first example (Figure 3), two radar sensors in remote locations need to have their data merged into a single signal processing engine. Each sensor presents analog data to an A/D converter, which makes the conversion to digital and sends the data to a PMC that is providing a Serial FPDP link back to the processing complex.

The advantages of this implementation are that the data can be captured and digitized close to the sensor, then shipped digitally over a Serial FPDP connection (up to distances of 30 meters using copper wires) for further processing at the signal processing board. Use of the Serial FPDP interfaces over a fiber optic connection allows distances up to 10 kilometers to be spanned if necessary. The Serial FPDP interfaces are also fast, running at 247 Mbytes/s. Once on the processor card, data is extracted from the Serial FPDP links and passed to the host via other serial link ports on the XMC connectors.

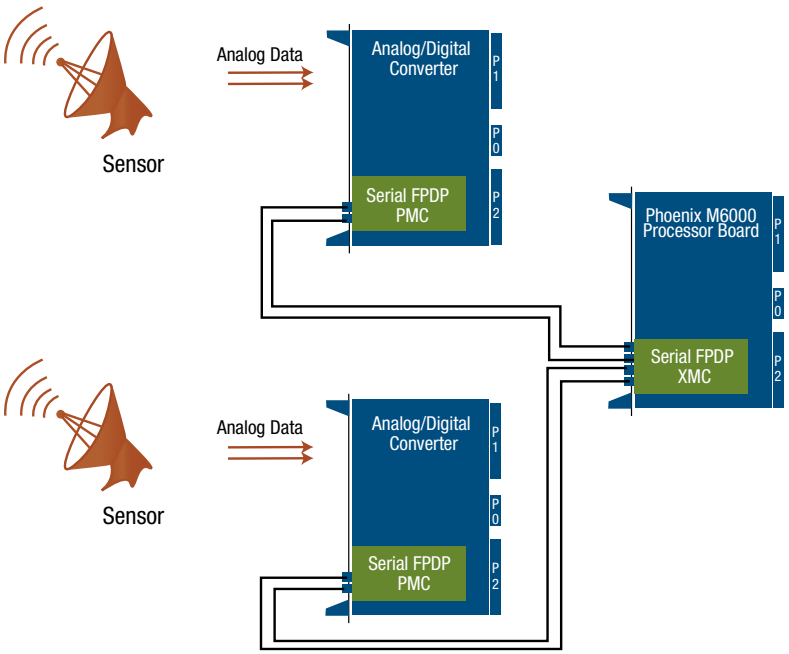

Figure 3

In this example, two radar sensors in remote locations need to have their data merged into a single signal processing engine. Each sensor presents analog data to an A/D converter, which makes the conversion to digital and sends the data to a PMC that is providing a Serial FPDP link back to the processing complex.

Very High-Speed Recording

In the second example, data is acquired on a very high-speed 10-bit A/D board gathering data at up to 2.5 Gbytes/s from a sensor (Figure 4). Once digitized, data is passed on to the VXS backplane for recording using three striped Fibre Channel data recorders to meet real-time bandwidth requirements.

The discussion has focused on point-to-point connections, but a switch is shown in this example. In this case, the switch is a crossbar, which enables multicasting from the single A/D converter to each of the three data recorder controllers. The switch is set up for a fixed configuration, and provides a minimum latency connection between the boards. The A/D board uses eight 1x links to pass data to the switch, which in turn multicasts over three sets of eight 1x links to the data recorder controllers.

Another point to note is the VXS backplane in this example. One advantage of the use of the backplane is to simplify connections—no cabling is required to transfer data on the backplane. Another is openness—any HSSI can be implemented as long as the communicating cards support it. In this case, the connections over the VXS links are implemented with Aurora.

Packing FPGAs to Save Space

For the third example, refer to Figure 2 again, which shows a sensor streaming data to an FPGA, which performed pre-processing and in turn streamed the pre-processed data to a CPU. FPGA implementations of point-to-point HSSIs make this system easy to construct. The sensor interface can be customized to the interface and speed required—perhaps using a standard Serial FPDP interface or a legacy interface with a custom protocol. Pre-processing of the data in the FPGA can decimate the speeds coming off the sensor into rates more suitable for general-purpose processing.

Once processed, data can then be passed to a CPU. The HSSI link out of the FPGA might be a general-purpose interface such as Serial RapidIO to interface to available parts on a wide range of processors. Or, if the "CPU" is in fact a second FPGA with a pro-

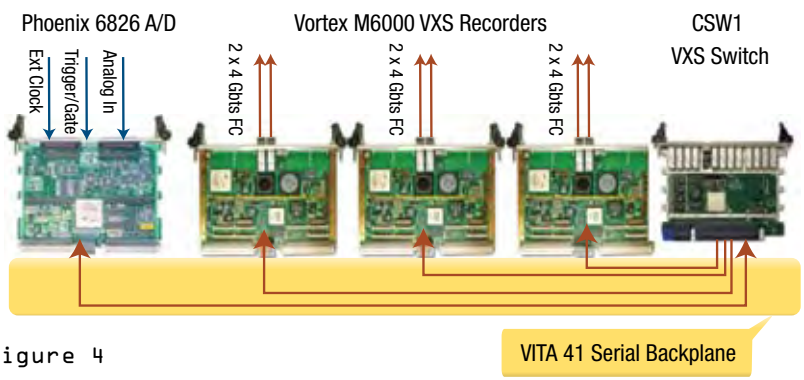

Figure 4

In this example, data is acquired on a very high-speed 10-bit A/D board gathering data at up to 2.5 Gbytes/s from a sensor. Once digitized, data is passed on to the VXS backplane for recording using three striped Fibre Channel data recorders to meet real-time bandwidth requirements.

cessor core, a protocol such as Aurora can be implemented. This architecture increases the flexibility of the physical implementation. The FPGA might reside on an XMC, with the CPU on a 6U VPX board. Or, there might be some distance between the FPGA—presumably close to the sensor—and the CPU board, spanned by a HSSI.

HSSIs Create Flexibility

In all three examples, an architecture using a high-speed serial interconnect creates flexibility for the designer. HSSIs allow designers to choose both the link type and the protocol that is best for the application, unlike when using a parallel bus and being locked into a protocol that may not be appropriate to each application.

HSSIs can be used for both I/O and "data plane" functions, meeting needs system-wide. In a point-to-point scenario, even more flexibility can be realized when the HSSI implementation is tuned, or even customized to meet specific requirements of a project. And if built in an FPGA, it can be quickly adapted for different requirements for the next project. As SerDes speeds continue to increase, HSSIs will become even more prevalent in system designs. They are a handy tool that should be in every military system designer's bag of tricks.

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RoHS Complicates Obsolescence Management, EOL

The effects of RoHS compliance have been added to other component obsolescence problems, and are having some unforeseen effects on EOL.

Ann R. Thryft
Senior Editor

Component obsolescence, often referred to as Diminishing Manufacturing Sources and Materials Shortages (DMSMS), can be tricky to manage. A growing infrastructure of companies and organizations are available to help military system designers cope with obsolescence and related issues. Over 30 of those players, and what they can do to help, are listed in *COTS Journal*'s "Eighth Annual End-of-Life Supplier Directory," following this article.

Both key DoD organizations and commercial firms involved in the problems of component obsolescence are included in the Directory, accompanied by a description of the services each provides. The three main DoD organizations listed are the Defense Microelectronics Activity (DMEA), the Defense Supply Center Columbus (DSCC) and the Government-Industry Data Exchange Program (GIDEP).

Today, components are going end-of-life for multiple reasons, and there are multiple ways of dealing with the problems that follow. Inventories of obsoleted devices are stocked by a number of after-market chip suppliers. Some of these are small firms that specialize in after-market business, while others are large distributors that include after-market products as part of their portfolios. Other firms may be packaging houses that custom assemble obsolete ICs using existing die and wafers.

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The RoHS Ripple Effect on EOL

One of the major new factors influencing obsolescence management is the effect of the global transition to lead-free substances in electronics manufacturing. Although military equipment is technically exempt from the European RoHS directive and similar initiatives, that status could easily change in the future. Meanwhile, related legislation is underway in Japan and China, and several U.S. states have passed, or are considering passing, similar legislation.

But even if military equipment retains its exemption, programs will be affected. The vast majority of commercial component electronics manufacturers and board makers supply both military products in smaller volumes, and much larger volumes of commercial products. A recent informal survey by *COTS Journal* of some vendors of board- and system-level electronics to the military, revealed that many suppliers still building leaded versions of their products have not yet encountered problems finding parts.

Most are regularly reviewing their bill-of-materials for each board-level product and have already made any necessary last-time buys for parts that are being obsoleted, although some vendors don't review BOMS for standard products regularly, but only when substituting new parts for obsoleted ones. Some components, such as "jellybeans," that are only made in RoHS-compliant versions can still be used in leaded, non-RoHS-compliant products as long as they work the same way; only the manufacturing process must be different.

But when manufacturers stop producing a particular technology and there isn't a RoHS-compliant replacement, that's when it becomes a major issue. In a few cases where a part has gone end-of-life, a board manufacturer either underestimated the need in a legacy product for replacement parts, or a customer didn't have enough funding to buy sufficient quantities to maintain stock levels.

An unforeseen ripple effect of the RoHS initiative on EOL is the rise in the number of counterfeit parts. As the effects of RoHS legislation have caused the obsolescence of an increased number of

components, the traffic in counterfeits of those components has also increased, with many of them originating in China. Counterfeit parts usually look exactly like the real thing, but may either function not at all, or only long enough to cause failures in the field.

In an effort to help with problems caused by counterfeits, as well as other aspects of obsolescence management including replacement parts, the Defense Sustainment Consortium (DSC) is expanding its presence in regional centers throughout the U.S. (see sidebar "Defense Sustainment Consortium Opens Regional Technology Centers"). The centers are a key part of the DoD's Competitive Sustainment Program, executed by the DSC, whose overall mission is to substantially reduce the support cost and improve the readiness of fielded weapons systems through innovative government/industry partnerships. ▮▮

Defense Sustainment Consortium Opens Regional Technology Centers

Better ways of managing obsolescence, better tools for locating replacement parts and technical innovations to combat the military's latest sustainment problems are needed to keep fielded weapons systems and aircraft ready for battle. Those needs are behind a recent decentralization move by the Defense Sustainment Consortium (DSC) to establish specialized regional and technology centers throughout the nation.

The centers will enable the DSC to achieve economies of scale and efficiency, as well as better manage operations. Each of the five existing or proposed centers (Figure 1) is located in a region with specific core competencies in a particular area of industry, such as aircraft engines.

The main goal of these centers is to help local companies, including larger defense contractors and OEMs, as well as emerging technology companies and government stakeholders, with specific technologies in each region. "The decentralization gives us a regional footprint that will help attract local and federal support in those areas," says Dale Karraker, DCS executive director. "Each area is also full of new businesses looking for new markets. When we open a center in a region, it helps leverage existing technologies to fix various problems of the government."

In January, the National Data and Integration Test Center (NDITC) hosted by ARINC Engineering Services in Annapolis, MD became the second DSC center. It will focus on activities to support aging aircraft, including obsolescence management, total life cycle management and the role of IT. In addition, the Annapolis center will combat the growing problem of counterfeit electronic parts, which are entering the supply chain in increasing numbers, says Walt Tomczykowski, ARINC's program director for life cycle management.

"This center is designed to encourage collaboration among large DoD stakeholders," says Tomczykowski. "Agencies and contractors will be able to try out new sustainment tools and this will directly benefit DoD weapons programs." The center will be an independent assessor of commercially available technology, as well as databases and other DoD sustainment products.

The first DSC center opened was the National Sustainment Technology Center in San Antonio, TX, focusing on corrosion, engines and airframe structures. Since January, the Defense Sustainment Engineering Sciences Center was established in Philadelphia, PA, and the Defense Sustainment Manufacturing Center opened in Pueblo, CO. A fifth center, the Defense Sustainment Legacy Electronics Center, has also been proposed.

ARINC Engineering Services
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(800) 633-6882.
[www.arinc.com].

Defense Sustainment Consortium
Charleston, SC.
(843) 760-4620.
[dsc.ati.corp.org].

Figure 1

The Defense Sustainment Consortium (DSC) is expanding its reach into five specialized regional and technology centers throughout the nation to help with obsolescence management, as well as other sustainment issues, of fielded weapons systems and aircraft. The DSC receives specific strategies and priorities from the Joint Council on Aging Aircraft (JCAA) and the Joint Aeronautical Commander's Group (JACG).

Source: Defense Sustainment Consortium

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Bus	AT Expansion Bus			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Universal Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	
	PCI Bus Masters	4	4	4	4	4	4	4	4	4	4		4	
	APIC (add'l PCI interrupts)	9	9	9	9	9	9	9	9	9	9			
CPU and BIOS	CPU Max Clock Rate (MHz)	1400	1400	1400	1400	400	650	400	650	400	650	333	333	333
	L2 Cache	2MB	2MB	2MB	2MB	256k	256k	256k	256k	256k	256k	16K	16k	16k
	Intel SpeedStep Technology	✓	✓	✓	✓									
	ACPI Power Mgmt	2.0	2.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0			
	Max Onboard DRAM (MB)	512	512	512	512	512	512	512	512	512	512	256	256	256
	RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Quick Boot Option Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IDE and Floppy Controllers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	ATA/IDE Disk Socket, 32 DIP	1	1	1	1	1	1	1	1	1	1	1	1	1
	Audio	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
	Digital Video	LVDS	LVDS	LVDS	LVDS			TTL	TTL	LVDS	LVDS	TTL	TTL	
	Analog Video	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	
	AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O	RS-232/422/485 Ports	2	1	2	1	2	2	2	2	2	2	2	2	2
	USB 2.0 Ports	2	4	2	4									
	USB Ports					2	2	2	2	2	2	2	2	2
	10/100Base-T Ethernet	1		1		1	1	1	1	1	1	1	1	
	ECP Parallel Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	aDIO(Advanced Digital I/O)	18	18	18	18	18	18	18	18	18	18	18	18	18
	multiPort(aDIO, ECP, FDC)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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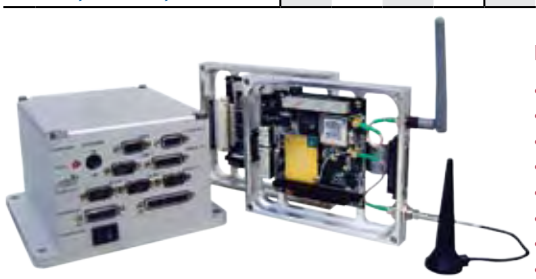

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Bus	AT Expansion Bus	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Expansion Bus Master	✓	✓				✓							✓	✓
	McBSP Serial Ports	✓	✓				✓								
Analog Input	Single-Ended Inputs	16	16	16	16	16	16								
	Differential Inputs	8	8		8	8	8								
	Max Throughput (kHz)	1250	1250	40	500	100	1250								
	Max Resolution (bits)	12	12	12	12	16	12								
	Input Ranges/Gains	3/7	3/7	3/1	3/4	1/4	3/6								
	Autonomous SmartCal	✓	✓												
	Data Marker Inputs	3	3		3		3								
Conversions	Channel-Gain Table	8k	8k		8k	8k	8k								
	Scan/Burst/Multi-Burst	✓	✓		✓	✓	✓								
	A/D FIFO Buffer	8k	8k		8k	8k	8k								
	Sample Counter	✓	✓		✓	✓	✓								
	DMA or PCI Bus Master	✓	✓		✓	✓	✓	✓						✓	
	SyncBus	✓	✓				✓								
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	48	18/9	32	64	32	48	48
	Bit Programmable I/O	8	8		8	8	8	8	24	6/0				48	✓‡
	Advanced Interrupts	2	2		2	2	2	2	2					2	
	Input FIFO Buffer	8k	8k		8k	8k	8k							4M	8M
	Opto-Isolated Inputs										16	48	16		
	Opto-Isolated Outputs										16	16			
	User Timer/Counters	3	3	3	2	3	3	3	3	3				10	6
	External Trigger	✓	✓		✓	✓	✓	✓	✓					✓	
	Incr. Encoder/PWM									3/9					✓‡
	Relay Outputs												16		
Analog Out	Analog Outputs	2	2		2	2	2	4							
	Max Throughput (kHz)	200	200		200	100	200	200							
	Resolution (bits)	12	12		12	16	12	12							
	Output Ranges	4	4		3	1	4	4							
	D/A FIFO Buffer	8k	8k				8k	8k							

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CALCE Electronic Products and Systems Center	College Park, MD. (301) 405-5323. [www.calce.umd.edu].	B, DB, R, S	Widely regarded as the industry's most knowledgeable source for evaluating and using components outside of OEM specifications. Also known for expertise in design refresh planning and other DMSM management activities, parts management and supply chain assessment for quality and reliability.
Chip Supply	Orlando, FL. (407) 298-7100. [www.chipsupply.com].	D, P	Offers semiconductor die and packaging solutions. Capabilities include post wafer fab processing, including dicing, inspection, engineering and test services; obsolescence management/life cycle planning; and specialized packaging solutions, including ceramic, CSP, TAB and QML.
CPU Technology	Pleasanton, CA. (925) 224-9920. [www.cputech.com].	B, E	Uses advanced design tools in developing system-on-a-chip-based technology to produce modernized, backward-compatible embedded computing solutions and high-performance, general-purpose multicore processors for use in military and commercial environments.
DMEA	McClellan Park, CA. (916) 231-1506. [www.dmea.osd.mil].	B, E, F, G, P	DMEA provides long-term, strategic support for the entire range of DoD systems that utilize microelectronics. DMEA uses a unique, innovative methodology to reverse-engineer microelectronic devices to determine their function and a specification; analyze possible solutions; and design, build, and test the best solution. An on-site reconfigurable foundry produces die in several critical process technologies.
DPA Components International	Simi Valley, CA. (805) 581-9200. [www.dpaci.com]. [www.dpems.com].	D, P, S	Specialty recovery process to remove and reuse die from OEM plastic or ceramic packaged parts, repackaging, upscreening and testing. Comes close to DMEA definition of "reclamation," but at a die level.
DSCC-VQ	Columbus, OH. (614) 692-0662. [www.dscc.dla.mil/offices/sourcing_and_qualification/].	DB, G, R	QML/QPL product for OEM procurement and logistics support to military services. Provides oversight of electronic component manufacturers for the military services.
Electronic Material Industries	Toluca Lake, CA. (818) 763-9584. [www.militarycomponents.com].	O	Buys, sells and stocks military and commercial electronic components.
Falcon Electronics	Commack, NY. (631) 351-8515. [www.falconelec.com].	L, O, S	Distributor to the avionics, military and space industry. Segregated product handling per JEDEC and MIL-STD. Offers DMS support services such as Global Semi Search and access to an extensive obsolete inventory. Also offers upscreening.

Company/Organization	Contact	Category	Comment
GD California	Livermore, CA. (925) 456-9900. [www.gdca.com].	B, E, O	Manufacturer specializing exclusively in legacy boards, system-level products and obsolescence management. Over 3,000 products include VME, CompactPCI, STD/STD32 and Multibus systems. Custom and COTS products are manufactured for industries including military, semiconductor, medical, telecom and industrial.
GIDEP	Corona, CA. (951) 898-3213. [www.gidep.org].	DB, G, R	The DoD's centralized database for DMSMS issues; hotlinks to numerous industry references on DMSMS. Host for the DoD DMSMS Knowledge Sharing Portal (DKSP).
IEC/IECQ	Geneva, Switzerland. +41 22 919 02 11. [www.iecq.org].	R	IEC generates international standards for the practice of uprating components and using them in systems. IECQ conducts the IEC's certification program for electronic components, processes and related materials, including aerospace.
IHS	Englewood, CO. (303) 397-2896. [www.IHS.com].	DB, L	4DOnline Parts Universe catalogs more than 14 million electronic parts from over 500 manufacturers in 350+ categories. HAYSTACK contains over 100 million parts in Federal Supply Catalog and over 40 U.S. Army, Navy, Air Force and related databases. Fasteners eCatalog enables identification, specification and sourcing of aerospace and defense standard fasteners/hardware.
Innovasic Semiconductor	Albuquerque, NM. (505) 883-5263. [www.innovasic.com].	E	A fabless semiconductor company that provides embedded solutions and replacement IC services for the long life-cycle market.
Inventory Locator Service (ILS)	Memphis, TN. (901) 794-5000. [www.ilsmart.com].	DB, L	Focuses primarily at the subsystem level.
L-3 Communications, Advanced Products & Design	San Diego, CA. (858) 597-9166. [www.L-3Com.com/apd].	B, E, P	Rapid Retargeting engineering services developer/provider for board-level electronic components and subsystems. Approach relies on reconfiguring hardware and software to be form, fit and functional replacements.
Lansdale Semiconductor	Tempe, AZ. (602) 438-0123. [www.lansdale.com].	D, E, O, P	Aftermarket support of over 3,000 obsolete ICs from Motorola, Philips, Intel, National, AMD and others. Manufactures products using the original tooling to ensure same performance and quality. QML certified to MIL-PRF-38535.
Maxwell Technologies	San Diego, CA. (858) 503-3300. [www.maxwell.com].	E, P	Uses MCM package as form, fit and functional replacement. Company's Rad-Pak technology enables commercial devices to meet space requirements. Fabless, QML-certified, with radiation testing and laboratory analysis capabilities.
Minco Technology Labs	Austin, TX. (512) 834-2022. [www.mincotech.com].	D, O, P	Semiconductor, processor and tester serving military, space and commercial industries.
MTI	Fort Walton Beach, FL. (850) 664-6070. [www.mtifwb.com].	B, DB, E, L, R	Obsolescence management software, engineering services, design, redesign and manufacturing.
NAPCO International	Hopkins, MN. (952) 931-2400. [www.napcointl.com]	B, DB, D, O, P, S	A global engineering, materials management, procurement, packaging, containerization and light manufacturing company specializing in the support of military tracked and wheeled equipment.
Now Electronics, N2O Semi Division	Huntington, NY. (800) 669-3532. [www.n2osemi.com].	L, O, P	Distributor specializing in all types of obsolete memory and specialty semiconductors. Provides support for legacy products from Dens-Pak, as well as support for DMS for White/EDI, IDT, Cypress, MOSAIC, APTA/HMP and Austin. Mil-Spec and other advanced packing and testing services available.
Pikes Peak Test Labs	Colorado Springs, CO. (719) 596-0802. [www.pptli.com].	B, D, E, L, O, P, S	Lab experienced in electronic component testing and evaluation, including environmental testing, destructive physical analysis, failure analysis. Also offers calibration services. Does high- and low-temperature testing and upgrade screening for commercial, industrial and military parts.

Company/Organization	Contact	Category	Comment
Precience	Silver Spring, MD. (301) 421-9054 [www.precience.com].	DB	Assists in up-front component selection, lifecycle prediction algorithm and EOL notification. Delivers environmental compliance management, component obsolescence and lifecycle management, content management and design chain management solutions. Provides data cleansing, as well as a RoHS data aggregation tool to speed compliance with product lifecycle management environmental health and safety implementations.
QP Semiconductor	Santa Clara, CA. (408) 737-0992. [www.qpsemi.com].	DB, D, E, F, R	QML manufacturer and supplier of high-reliability hermetic ICs for military, aerospace and industrial applications; solutions for DMSMS and EOL problems.
Richardson Electronics	LaFox, IL. (630) 208-3637. [www.rell.com].	DB, O, P	Distributor serving RF and wireless communications, industrial power conversion and medical imaging markets. Engineering services are available to aid product manufacturing, systems integration, prototype design and parts logistics from design-in through after-market stages.
Rochester Electronics	Newburyport, MA. (978) 462-9332. [www.rocelec.com].	D, F, O, P, R	Authorized/franchised supplier of aftermarket parts for over 40 semiconductor suppliers with over 500 million finished parts and 3 billion die. Manufactures over 15,000 aftermarket devices, from commercial to fully certified military. Offers packaging and testing to extend product life even further.
Sarnoff	Princeton, NJ. (609) 734-2168. [www.gemes.com].	B, E, F, R, P	Government-authorized contractor for Generalized Emulation of Microcircuits (GEM) program.
Sensitron Semiconductor	Deer Park, NY. (631) 586-7600. [www.sensitron.com].	B, D, E, F, P, R, S	Full-service provider including R&D, design, wafer fabrication, packaging, screening, testing and engineering. Maintains a wafer fabrication clean room and a microelectronics manufacturing clean room.
Sypris Test and Measurement	Orlando FL. (800) 839-4959. [www.wetest.com].	S	Offers test and calibration services to space and defense prime contractors, government agencies and commercial manufacturers, including automotive, avionics, telecom and medical. Services include semiconductor and passive component test, wafer probe, product test and evaluation, and repair and calibration of general electrical and mechanical test equipment. Fixed locations, on-site locations and mobile calibration facilities nationwide. ISO-9001:2000 registered, DSCC-approved, A2LA (ISO/IEC-17025) accredited and ISTA-certified.
T.S.I. Microelectronics	Danvers, MA. (978) 774-8722. [www.tsimicro.com].	D, E, O, P	Manufactures custom thick and thin film hybrids to SCDs for DSCC and military OEMs. Offers custom IC packaging into hermetic packages. Design and reverse engineering; second source to various obsolete hybrid circuits and discrete semiconductors.
Total Parts Plus	Fort Walton Beach, FL. (850) 244-7293. [www.totalpartsplus.com].	DB	Internet obsolescence and material content databases for all grades of semiconductors as well as database enhancement services.

Abbreviation	Categories	Explanation
B	Board level	Solves board-level DMS problems (as opposed to component-level problems).
DB	Database	Provides a database covering topics such as alternate sources, devices that are obsolete, cross-references or uprating results.
D	Die processor	Refers to processing OEM die, not an emulated solution.
E	Emulation/reverse engineering	Vendor may emulate a DMS device in a gate array or full-custom device, or provide a pseudo-form, fit and functional equivalent.
F	Foundry	Has foundry capability to fabricate wafers
G	Government agency	—
L	Locator	The vendor provides a service to locate DMS components and boards/systems.
O	Obsolete inventory	Maintains OEM inventory in die or packaged form.
P	Specialty packaging	Packages components as monolithic or multi-chip modules.
R	Industry reference	Denotes an organization or company with widely recognized knowledge or information concerning the DMS industry.
S	Uprating/upscreening	Performs uprating or upscreening.

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Technology Focus

FPDP I&II and Serial FPDP Boards

FPDP and Serial FPDP Enlist for High Bandwidth Duties

FPDP and its newer counterpart Serial FPDP offer a simple, low-overhead interface scheme for high-bandwidth, point-to-point data transfers.

Jeff Child
Editor-in-Chief

The Front Panel Data Port (FPDP) interconnect standard has proven itself as an effective solution for high-throughput point-to-point data movement. It's particularly useful in military applications like radar and sonar where FPDP is used as the interface to sensor networks. Because FPDP operates independently of the backplane bus, it provides a deterministic sustained bandwidth free from contention.

Implemented with a low-cost ribbon cable, FPDP links boards without eating up more than a tiny amount of board space. Because FPDP does not require a host computer at the sensor end, processing overhead is reduced to the bare minimum, allowing for maximum data throughput. But more importantly, the elimination of the host computer means there are none of the complications inherent in having an operating system manage data transfer details.

FPDP's younger cousin Serial FPDP (ANSI/VITA 17.1-2003) goes a step further by nullifying the distance limitations of FPDP. Instead of a connection, it uses a serial interface based on the Fibre Channel physical layer. Serial FPDP retains the frame format of the original standard thus simplifying the exchange of data between parallel and serial implementations. That permits the easy exchange of data from local chassis and legacy systems using parallel interfaces to remote chassis through a Serial FPDP connection. The ANSI/VITA 17.1-2003 specification for Serial FPDP supports 1 Gbit/s, 2 Gbit/s and 2.5 Gbit/s link speeds. A more recent version, FPDP II, provides data rates up to 400 Mbytes/s and has found some acceptance even though it's not an official standard.

Compared to PCI Express for example, which can chew as much as 40 percent of host processor or FPGA's resources, Serial FPDP uses as little as one percent. The addition of an optical connection to the physical layer provides better noise immunity and extended range with distances of up to 10 km being supported by the standard. Future versions of the protocol will support data rates of up to 10 Gbits/s and will be standardized as ANSI VITA 17.2.

Sonar is among the key applications that have used FPDP, including such major sonar upgrade programs as the SQQ-89 sonar upgrade for the guided missile (DDG) class of destroyers, the sonar for the New Attack Submarine (NSSN) and the P3 Aircraft. The SQQ-89 Sonar transmit and receive systems are used on Arleigh Burke Class (Aegis) Guided Missile Destroyers such as the USS McCampbell (Figure 1). The sonar suite aboard the vessel class is the Lockheed Martin SQQ-89(V)6, which includes Edo Corporation AN/SQS-53C bow-mounted active search and attack sonar and the AN/SQR-19B passive towed array. The suite is reportedly being upgraded to SQQ-89(V)15 to allow deployment of the Lockheed Martin AN/WLD-1 Remote Minehunting System.

Until last year, few bus analyzer tools were available for Serial FPDP. The first to emerge is the Axiom Series from Absolute Analysis. At the heart of the Axiom Series is the advanced Protocol Analyzer Engine with speeds up to 4.0 Gbits/s, which is combined with the company's Investigator software applications. The tool does full line-rate capture of Serial FPDP traffic. Data is displayed in frame, word, 10b, 8b and K/D views. The analyzer provides real-time statistics and frame-building traffic generation with error injection. ▮▮

Figure 1

FPDP is used in sonar upgrade programs like the SQQ-89. Sonar transmit and receive systems are used on Arleigh Burke Class (Aegis) Guided Missile Destroyers such as the USS McCampbell (DDG 85). The vessel is shown here last summer as it executes a high-speed maneuver, during a sea power demonstration while on deployment in the Pacific Ocean.

(DoD photo by MCSN Kathleen Gorby, U.S. Navy).

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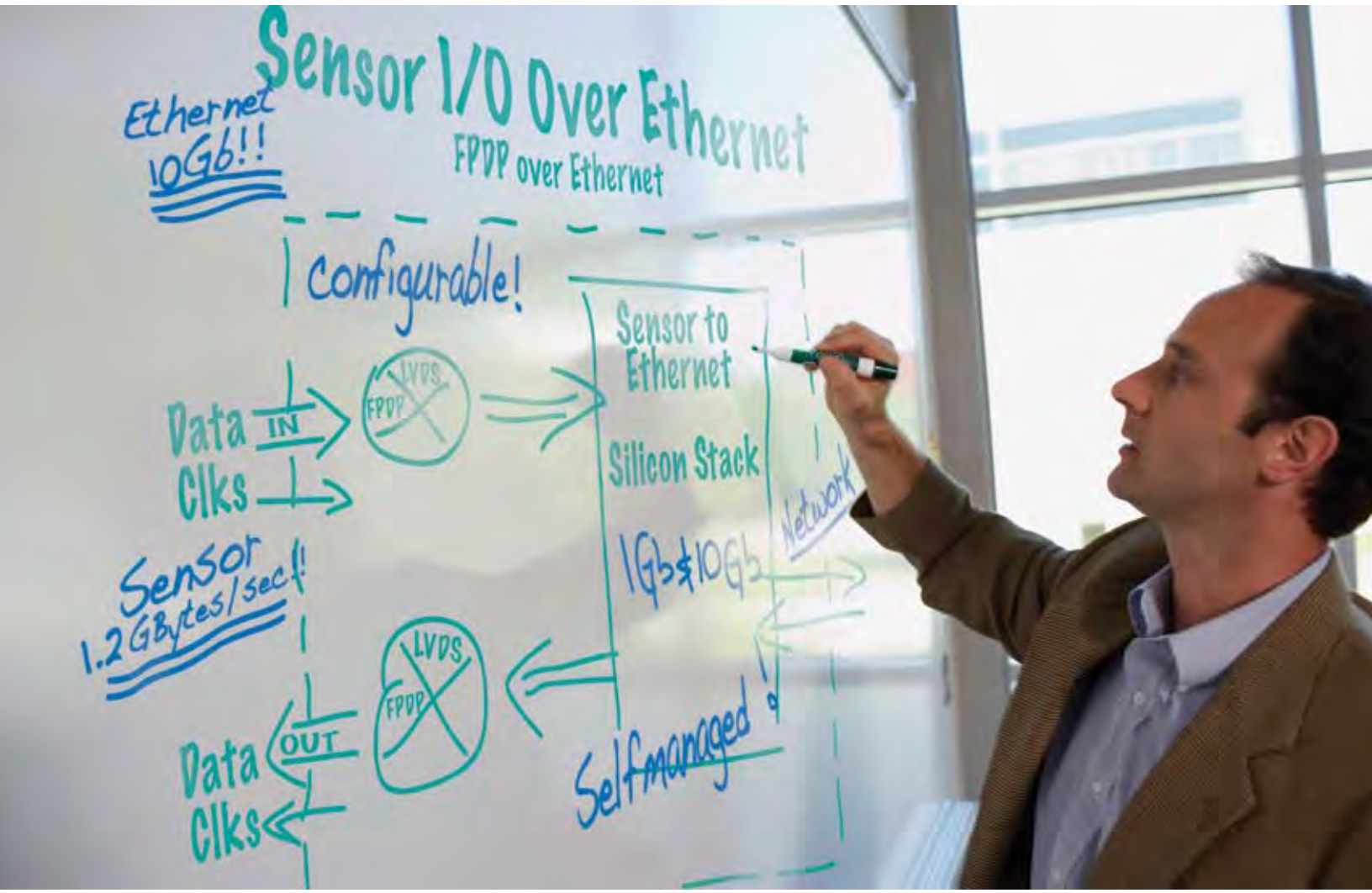

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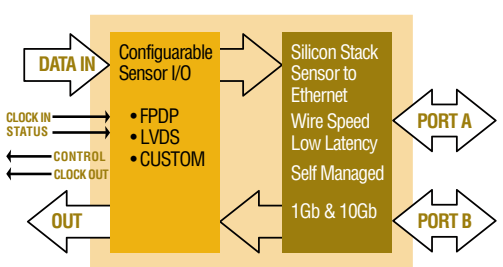

CRITICAL I/O

www.criticalio.com

Technology Focus:

FPDP I&II and Serial FPDP Boards Roundup

Card Delivers 3.125 Gbits/s on Four Ports

It's not always possible to get data conversion gear close to where the analog data is acquired. Serial FPDP is rapidly becoming the interconnect of choice for streaming data capture systems because it is a protocol optimized for maximum data rates and minimum overhead. It efficiently accommodates many applications requiring great distances between the data input site and

data processing stations. Along those lines, Conduant offers its StreamStor Serial FPDP Mezzanine Board for long-distance, high-speed, data capture from Serial FPDP or other optical fiber data protocols. When combined with Conduant's StreamStor Amazon SATA disk controller, real-time data input performance exceeds 500 Mbytes/s.

The StreamStor Serial FPDP Mezzanine Board features four independent optical fiber interface ports for simultaneous data input and output available on each port. With data rate and wavelength options, the board can support cable lengths up to 25 kilometers. The StreamStor Serial FPDP Mezzanine Board exceeds the ANSI/VITA 17.1-2003 specification with sustained rates of 300 Mbytes/s (3.125 Gbytes/s). Wavelength options include 850 nm (nanometers) and 1300 nm for distances up to 25 kilometers. Data rates range from 1.06-3.125 Gbits/s on each of the four ports. The mezzanine board supports multiport recording whether bonded or independent. It is field-upgradeable and features customizable hardware.

Conduant
Longmont, CO.
(303) 485-2721.
[www.conduant.com].

Serial FPDP Blends Point-to-Point and Broadcast Roles

The FPDP protocol was specifically invented to address the high-speed connection between the A/D converter of a sensor subsystem and the DSPs used in advanced image processing systems. The serial version of FPDP does that more effectively by extending the FPDP connection from 1m to 10 km while retaining its simplicity, bandwidth and reliability. Systran, now part of Curtiss-Wright, invented Serial FPDP, and their offering is the FibreXtreme SL100/SL240 Serial FPDP data link system that connects distributed devices through the VITA 17.1-2003 FPDP communications protocol. FibreXtreme is a dedicated, Point-to-Point or Broadcast Data Link consisting of a transmitting card (source) and one or more receiving cards (destination). Cards are bidirectional, capable of performing both functions simultaneously.

The SL240 Series operates at 2.5 Gbits/s, resulting in sustained throughputs up to

247 Mbytes/s. The SL100 Series, operating at a 1.062 Gbit/s baud rate, offers sustained data throughput of 105 Mbytes/s. Other FibreXtreme features include various levels of error detection and status reporting and 32 Kbyte source and destination FIFOs to absorb bursts. The product families include PCI, PMC and CPCI source and destination cards with dual DMA controllers and PIO for data transfer over PCI. FibreXtreme data link products are available in configurations designed to handle extremely harsh environments that subject system components to additional shock, vibration and humidity, and extended temperature ranges.

Curtiss-Wright Controls Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

XMC Brings Dual Serial FPDP to Sensor I/O

Mercury Computer Systems' Sensor I/O XMC daughtercard provides a direct interface into the RapidIO switch fabric for sensor input, enabling low-latency processing of data streaming directly from sensors. The daughtercard implements the Serial Front Panel

Data Port (Serial FPDP) protocol over fiber on two 2.5 Gbaud full-duplex channels.

Full system performance is enhanced because each channel can be programmed for data distribution without processor intervention. The interface can sense signals in the data stream that indicate sensor mode changes, and route data appropriately to different processors or endpoints on the RapidIO switch fabric. The board supports connections up to 150m and a real-time latency as low as 4 microseconds. All four FPDP data modes are supported, and it provides four DMA engines with chaining and branching. Support for Serial FPDP is as specified by VITA 17.1-2003 and is compatible with all products supporting any subset of the VITA 17.1-2003 protocol.

The Sensor I/O XMC is software-compatible with RACE++ Series RINOJ-F products, easing migration from the legacy I/O daughtercards while offering significant improvements in speed as well as configuration flexibility. The card draws approximately 6.5W of power (typical) and operates over temps of 0° to 40°C and at altitudes of 10,000 ft. A rugged version of the product is also available.

Mercury Computer Systems
Chelmsford, MA.
(978) 256-0052.
[www.mc.com].

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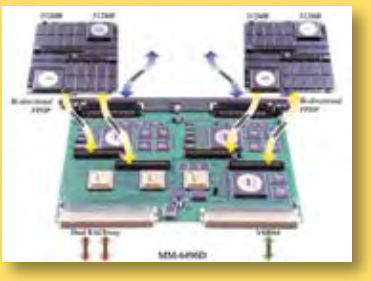
2 Gbytes of FPDP-Accessible Memory Ride VME

The point-to-point nature of FPDP makes it a popular solution for linking to large memory arrays. Exemplifying that trend, Micro Memory's MM-6496D product is a high-speed, nine-port, single-slot VME memory buffer that provides up to 2 Gbytes of DRAM for FPDP, VME and RACEway systems. Data from two independent FPDP ports and two independent RACEway ports can be directly transmitted or received from any one of four "non-busy" RACEway ports at 160 Mbytes/s with a combined data rate of 640 Mbytes/s.



In addition to having two FPDP ports and a VME port, the card has two RACEway ports on P2 and four RACEway ports on the face of the board. Each of these four ports has an individual memory bank with up to 512 Mbytes of DRAM. Each memory bank can be accessed simultaneously, but only through its dedicated RACEway port. The FPDP ports are controlled by a full chain DMA in the RACEway interface and can be initialized by a host processor on either the VME bus or over the RACEway. Reliability is ensured by burn-in and running memory diagnostics that check operations for 48 hours while temperature-cycling boards from 0° to 60°C.

Micro Memory
Chatsworth, CA.
(818) 998-0070.
[www.micromemory.com].

VME Digital Receiver Targets Software Radio

Developers of real-time DSP and software radio systems often want to avoid the lengthy, complex programming that can accompany the use of FPGAs. With the GateFlow Model 6821-422 high-speed A/D digital down-converter (DDC) board from Pentek, now they can. The board includes a factory-installed wideband digital down-converter FPGA IP core operating at frequencies of up to 296 MHz. It is a highly optimized, dual-channel version of Pentek's GateFlow IP Core 422 tailored to the board's various resources. The result is a preconfigured, fully tested digital software radio subsystem that accepts a front-panel analog RF input and delivers real or complex digital output samples translated to baseband from any frequency slice of the input signal. The board has a 12-bit sample rate at 215 MHz and four sets of user-programmable FIR coefficients for custom filtering.

The digital output signals are available on two or four FPDP connectors using several data-packing modes. In addition, the signals can be delivered as low voltage differential signaling (LVDS) through either the VMEbus P2 connector or a second-slot front-panel mezzanine.

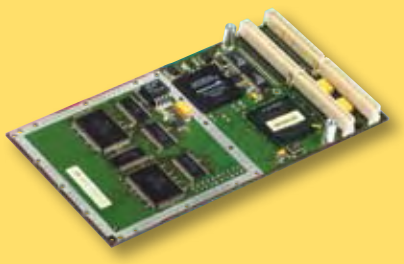
The Model 6821-422 is supported by Pentek's C-callable ReadyFlow Board Support Libraries. ReadyFlow provides development

tools for quick startup through application completion, allows programming at high, intermediate and low levels to meet various needs, and includes complete source code for all functions. Ruggedized and conduction-cooled versions of the board are available. Pricing starts at $17,495.

Pentek
Upper Saddle River, NJ.
(201) 818-5900.
[www.pentek.com].

PMC Brings FPDP II to Rugged Apps

Demand is on the rise for multichannel, high-rate sensor data transfer across a single backplane. Providing a solution, GE Fanuc Embedded Computing offers the ICS-8500, the first PMC to become available that delivers 400 Mbyte/s FPDP II—compared with 160 Mbytes/s for FPDP—in a rugged environment. The ICS-8500, which can be configured as either a transmitter or a receiver, also features 8 Mbytes of swing buffer memory, setting it apart



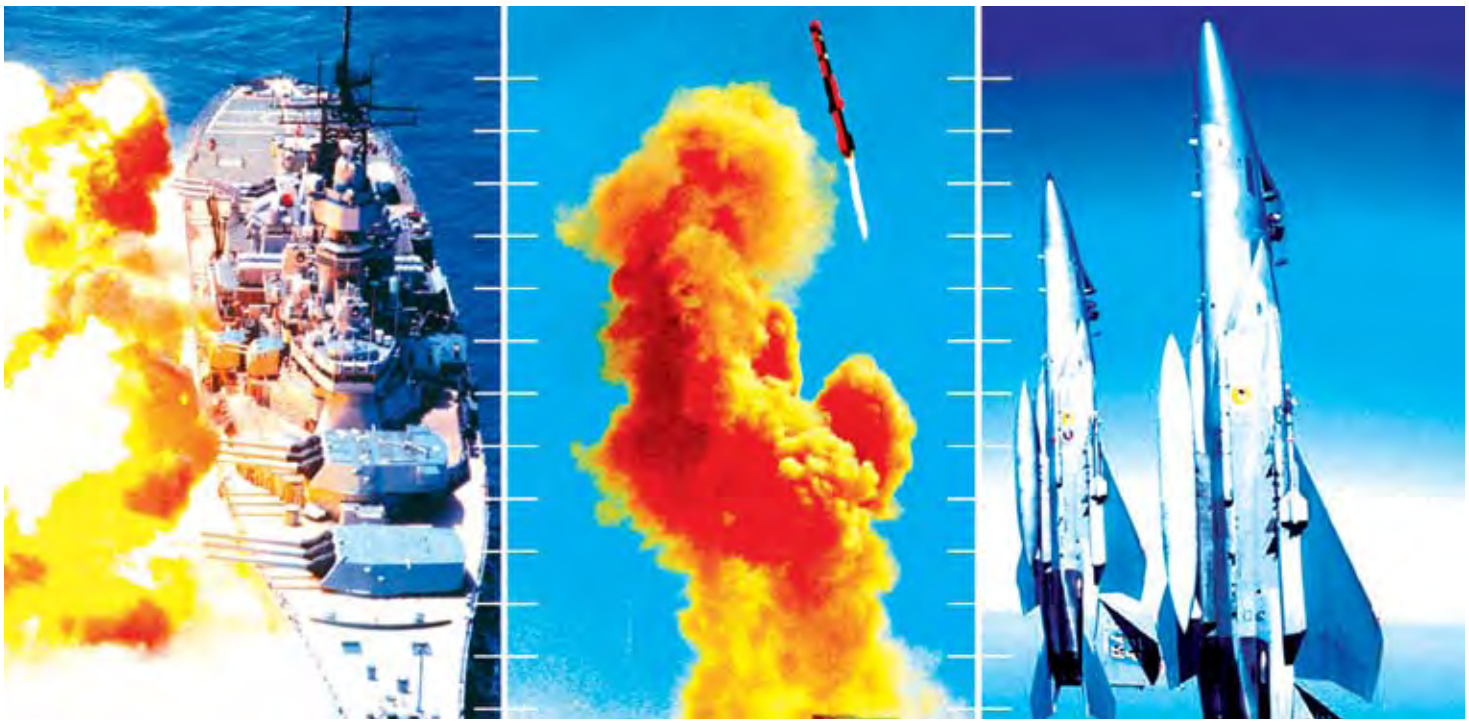
from products that provide only limited FIFO capability.

Available in convection- and conduction-cooled versions, the ICS-8500 offers similar functionality to the popular ICS-500-R and ICS-500-T PMC products, but is configurable under software control as either a receiver or transmitter. The 400 Mbytes/s FPDP II interface is provided via the P4 connector: when the ICS-8500 is communicating with a non-FPDP II device, it automatically reverts to ANSI/VITA 17 FPDP operation at 160 Mbytes/s.

In transmit mode, the board provides an FPDP/TM interface. In addition to a continuous data transmit capability, a Loop mode of operation is available, in which a fixed length of data equal to the programmed buffer length is written to both banks of the swing buffer. When triggered, this data is repetitively generated and transmitted by the FPDP output interface. In receive mode, the board provides both Receive (FPDP/R) and Receive Master (FPDP/RM) capabilities. A key feature of the product is its ability to perform the corner turning function: this software-enabled feature reorders multichannel data from channel ordering by time to time ordering by channel.

GE Fanuc Embedded Systems
Albuquerque, NM.
(505) 875-0600.
[www.gefanucembedded.com].

GE Fanuc
Embedded Systems



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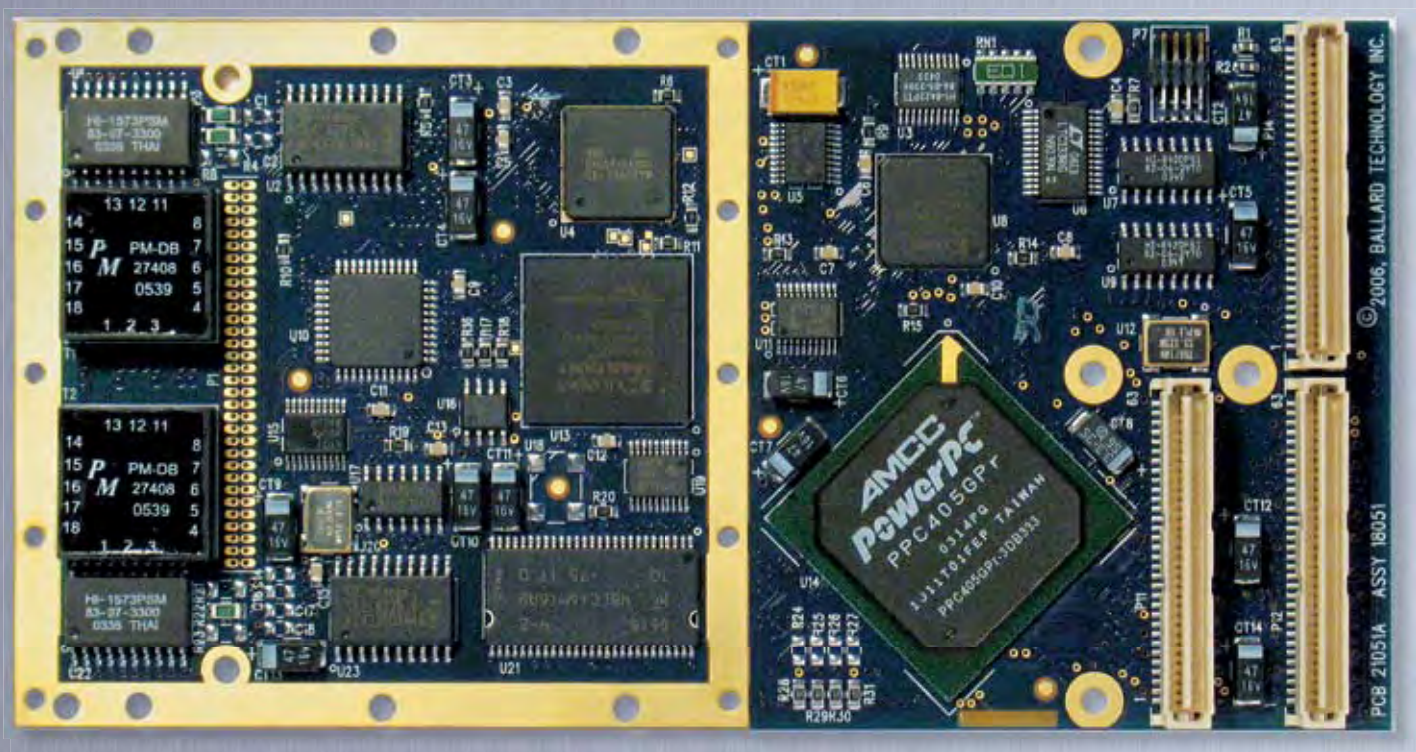

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Serial FPDP PMC Is Protocol-Agnostic

There's no doubt that FPGAs open up a treasure chest of flexibility for designers of I/O subsystems. Using FPGAs, designers can facilitate dropping in blocks of pre-integrated signal processing cores, thereby leveraging single hardware architecture across multiple applications. Following exactly that road, TEK Microsystems came out with the JazzFiber PMC, the first protocol-agnostic fiber optic PMC I/O module optimized for both streaming I/O and signal processing applications. The JazzFiber Quad Serial FPDP PMC module was the first member of Tekmicro's new family of JazzFiber FPGA-based multiprotocol fiber optic I/O modules. The JazzFiber PMC combines the advantages of the ANSI/VITA 17.1 Serial FPDP interconnect with highly integrated FPGA technology.

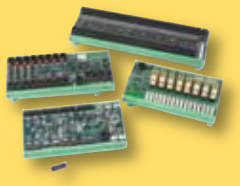
The use of a common FPGA architecture and software API allows applications to easily migrate between different JazzFiber solutions. The first JazzFiber protocol core supports ANSI/VITA 17.1 Serial FPDP. The JazzFiber PMC provides four fiber optic transceivers operating at up to 3.125 Gbits/s each, which can be configured as four independent interfaces or combined into a single 4x link. The JazzFiber PMC supports both PCI and PCI-X protocols at

up to 133 MHz. A full gigabyte of onboard DDR SDRAM allows deep buffering of streaming data at the full 1 Gbyte/s data rate. Pricing starts at $7,995 for two-channel models and $9,995 for four-channel models in single unit quantities.

TEK Microsystems
Chelmsford, MA.
(978) 244-9200.
[www.tekmicro.com].

VME Blade Sports Serial RIO and Serial FPDP Links

Intensive signal and data processing systems such as radar and imaging equipment place high demands on high-performance, low-latency throughput. Feeding such needs, Thales Computers offers its PowerNode5, the first dual 64-bit PowerPC970 VME blade server with backplane Serial RapidIO and Serial FPDP connectivity. The board is a rugged 6U VME PowerPC blade server featuring two 64-bit PPC970s running at 1.6 GHz. Its design is a clone of the IBM JS20 blade computer, providing the PowerNode5 with a very high level of performance



and full binary compatibility with IBM JS20 blade servers, in a 6U form-factor fully adapted to any of today's embedded systems requirements.

Thales' Serial RapidIO switch fabric is an original implementation with a distributed Serial RapidIO architecture: each PowerNode5 is equipped with a 4-port switch allowing a flexible, full-mesh interconnect of up to 4 PowerNode5s and scalable up to a 16-PowerNode5 machine. The PowerNode5 features triple x4 Serial RapidIO links available on an enhanced performance P0 connector, compliant with legacy VME64x backplanes. The PowerNode5 is also available with a twin Serial RapidIO link plus a single Serial FPDP link option. The current version of PowerNode5 blade computing node is currently shipping with an entry-level unit price of $9,670.

Thales Computers
Edison, NJ.
(732) 494-1011.
[www.thalescomputers.com].

Quad Serial FPDP Climbs Aboard XMC/PMC

FPDP offers many advantages as a point-to-point data link, and Serial FPDP does the same only faster. VMETRO expanded its range of high-performance PMC/XMC modules with the SFM Quad Serial FPDP module. The SFM supports up to four simultaneous serial FPDP (VITA 17.1-2003) channels. Until now, Serial FPDP cards have typically had just one channel. This new four-channel interface card provides a higher level of functional density without creating a bottleneck getting the data to and from the baseboard. The functional density and high performance is especially important for high-performance data recorders, high-channel density sensor arrays and high-end DSP systems. The simplicity and wide support for Serial FPDP make it ideal for a wide range of real-time embedded computer solutions.

In order to achieve optimal performance, VMETRO implemented the SFM with separate

DMA controllers for each channel. The SFM PMC module supports PCI-X data transfers at speeds up to 133 MHz. The SFM XMC module supports PCI Express via the XMC connectors and provides the full 2.5 Gbit/s data rate per channel. Using PCI-X and PCI Express this way enables more than one Serial FPDP transfer to happen simultaneously.

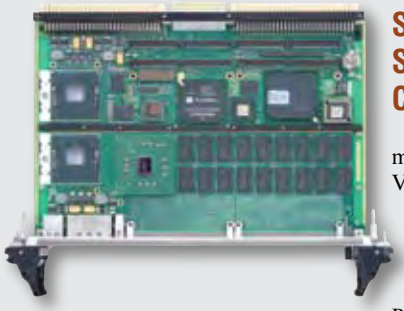
VMETRO
Houston, TX.
(281) 584-0728.
[www.vmetro.com].

Programmable Automation Controller Targets UAVs, ULVs

A new family of Linux-based, programmable automation controllers (PACs) targets ULVs and UAVs with compact size, ruggedness and flexibility. The UEIPAC series from United Electronic Industries includes an embedded computer running standard Linux, two Ethernet ports, a serial port, an SD Card interface, an inter-PAC sync interface and three or six slots for I/O boards. It has been tested from -40° to +85°C, at 5g vibration, 50g shock and at up to 70,000 feet. Applications deployed on the UEIPAC can run fully stand-alone, allowing smaller, faster, more reliable and higher-performance systems than are possible with an external host computer, as well as eliminating the cost of a dedicated host PC and guaranteeing long-term availability of the identical hardware.

Up to three I/O boards can be installed in the UEIPAC 300. Slightly larger at 4-in. x 4.1-in. x 5.8-in., the UEIPAC 600 allows the installation of up to six I/O boards containing up to 150 analog inputs or 288 digital I/O. I/O boards can include analog input, analog output, digital I/O, counter/timer, quadrature Encoder, serial I/O, CAN bus and ARINC-429 interfaces. The UEIPAC 300 is priced at $1,495 and the UEIPAC 600 at $1,795.

United Electronic Industries, Canton, MA. (781) 821-2890. [www.ueidaq.com].



Server-Class VME SBC Has Twin Dual-Core CPUs

The first server-class, manageable, 6U single-slot VME SBC that features a dual-core processor and board management controller has just doubled its processing power. The PENTXM4 from Thales Computers has two dual-core Intel 1.67 GHz Xeon ULV processors, compared to the company's PENTXM2 board, introduced last year. It comes with the Intel E7520 server-class memory controller hub, 2 Gbytes of DDR2-400 SDRAM and an onboard 4 Gbyte flash disk drive, and is targeted toward symmetrical processing systems.

The board's VITA 38 intelligent platform management interface (IPMI) feature provides for easy scaling into a multiprocessing system. Interfaces include a dual SATA-150 port, a triple USB 2.0 port and EIDE. The PENTXM4 runs Red Hat Linux and features an extensible firmware interface (EFI) BIOS/firmware that boots Linux 2.6, VxWorks, LynxOS, Microsoft Windows and Red Hat Linux Enterprise.

Thales Computers, Raleigh, NC. (919) 231-8000. [www.thalescomputers.com].

Ultra-Small Modem Module Sports RJ-11 Connector

A built-in, standard RF-11 phone jack can be handy for all kinds of embedded military applications that need data communications capabilities, and it's even more useful when combined with a modem. A new modem module that includes an RF-11 jack is aimed at small-footprint designs, measuring only 0.66 in. wide x 1.25 in. deep x 0.75 in. high. The TinyModem from Radicom Research includes data, fax and voice capability, as well as improved EMC/EMI shielding. It features a built-in data pump and a modem controller and tolerates high isolation voltages of up to 3750V, as well as low power consumption from a single 3.3V supply, 5V-tolerant I/O and sleep mode support.

Standard features include a serial TTL interface, onboard International DAA, AT command set support, caller ID type I and II for select countries and call waiting, as well as detection of line-in-use, remote hang-up and extension pickup. Also included are downstream data rates of up to 56 Kbits/s, a 14.4 Kbit/s fax rate and voice playback and recording capability. Prices begin at $29 in quantities of 1,000 or more.

Radicom Research, San Jose, CA. (408) 383-9006. [www.radi.com].

TCP/IP Stack Supports Dual-Mode IPv4/IPv6 Traffic

As DSPs are used in increasingly complex military network environments, TCP/IP is becoming an integral part of the total DSP solution, especially when Gigabit Ethernet is the local interconnect for DSP farms. In recognition of that fact, Enea has released DSPNet, a compact, high-performance TCP/IP stack for its OSEck DSP RTOS. The new stack is optimized for deeply embedded applications with tight size and cost constraints, and occupies less than 40 Kbytes of memory.

DSPNet supports IPv4, IPv6 and dual-mode IPv4/IPv6 traffic, as well as raw IP/UDP/TCP BSD Sockets, and provides a zero-copy API based on BSD Sockets. OSEck (OSE Compact Kernel) is a DSP-optimized version of Enea's full-featured OSE RTOS that occupies less than 8 Kbytes of memory in a minimal configuration. DSPNet will initially be available for OSEck running on Texas Instruments' C64x DSP family and Freescale's Starcore family. Pricing starts at $5,000.

Enea, San Jose, CA. (408) 383-9480. [www.enea.com].

Extended Temp COM Express Module Withstands -25°C

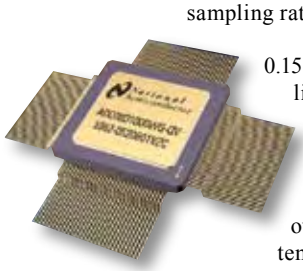
The PICMG COM Express standard gives designers the ability to plan for feature changes, demand fluctuations and performance upgrades without having to re-design their products each time, a big plus for military applications. A Com Express module series from RadiSys is designed for military applications that require extended temperature operation in conditions outside the standard 0° to 55°C window of existing COM Express modules. Based on the Intel Pentium M processor LV 738 running at 1.4 GHz, the CE738-E's fanless solution is designed for ruggedized transportation and military applications.

The CE738-E features the Intel 915GM chipset, the Intel ICH6M I/O Hub, a Type 2 COM Express pin-out, an Intel 82573 10/100/1000BaseTX Ethernet controller and a SODIMM socket for up to 1 Gbyte of memory. Ports include eight USB, two SATA and one ATA 100, as well as eight GPIO lines. The module's 32-bit/33 MHz PCI bus supports up to four logical devices. Software support includes Windows XP, Windows XP Embedded and Red Hat Desktop Linux.

RadiSys, Hillsboro, OR. (503) 615-1100. [www.radisys.com].

Low-Power, Rad-Tolerant, A/D Converter Targets Comsats

As one of the key signal-path building blocks in comsat systems, A/D converters must deliver superior signal-to-noise and distortion performance at the lowest power. An 8-bit, 1 Gsamples/s, dual-CMOS A/D converter chip from National Semiconductor delivers these characteristics, as well as only 800 milliwatts per channel power consumption. The ADC08D1000WG-QV is qualified for use in broadband and high-speed comsat applications and meets space-grade radiation tolerance levels of 120 MeV for single event latch-up and 300K rad (Si) for total ionizing dose. Using fully programmable, dual-edge sampling, the chip can achieve 2 Gsamples/s from one channel by interleaving both on-chip converters. A 1:2 demultiplexer feeds two LVDS buses, reducing the output data rate on each bus to half the sampling rate.



The ADC08D1000WG-QV achieves 0.15 least significant bits differential non-linearity, while maintaining a high 7.4 effective number of bits at an input frequency of 498 MHz (Nyquist). It has an extremely low bit-error rate of 10^{-18} and guarantees "no missing codes" over its extended -55° to 125°C operating temperature range. An on-command calibration mode prevents single event effects from triggering unwanted calibrations. It is available in a 128-lead multi-layer ceramic quad flat package and is space-grade qualified to MIL-STD-38535 QML level V. It can also be purchased as the standard military drawing 5962-0520601VZC.

National Semiconductor, Santa Clara, CA. (800) 272-9959. [www.national.com].

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3U PXI Express Smart Chassis Has Nine Slots

By utilizing PCI Express as a bus, PXI Express opens up multiple, higher-bandwidth design possibilities for military test and measurement and data acquisition applications. Taking advantage of that fact, Geotest-Marvin Test Systems has released the GX7600 series of nine-slot PXI Express Smart Chassis. The 3U chassis can accommodate up to eight instruments, as well as an embedded, single-slot PXI Express controller or a PXI Express remote bus controller. It incorporates onboard per-slot temperature and power supply monitoring.

The GX7600 has two PXI Express hybrid slots, five PXI slots and a PXI Express system timing slot, as well as a 400 watt power supply. Built-in peripherals, including a hard disk drive and a DVD-RW drive, are options for embedded controller configurations. The chassis' high-performance cPCI Express bus architecture delivers up to 1 Gbyte/s dedicated slot bandwidth and 3 Gbyte/s system bandwidth. The GX7600 series is available in both slave and master configurations. Pricing for the series ranges from $2,195 for the GX7610 nine-slot Smart 3U PXI Express Slave chassis to $3,195 for the GX7600-500 nine-slot Smart 3U PXI Express Master Chassis with hard disk drive, a DVD-RW drive and a 550W power supply.

Geotest-Marvin Test Systems, Irvine, CA. (949) 263-2222. [www.geotestinc.com].

Low-Noise Crystal Oscillator Has Low Profile

Applications that utilize phase-locked microwave signal sources, such as dielectric resonator oscillators (DROs), test equipment, microwave communication systems and military and doppler radar, demand superior noise performance. An ovenized, 100 MHz crystal oscillator (OCXO) from Bliley Technologies supports those applications with low noise in low-profile (0.53-in. maximum height) packaging. The NV45G1480 OCXO offers carefully matched crystals and oscillators to achieve optimal performance for noise, packaging nearly 50% smaller than previous generations of similar products, low power consumption and tight stability.

Typical phase noise is -130 dBc @ 100 Hz offset, stabilities are as tight as +/- 50 ppb over temperature, power consumption is 1 watt typical at 25°C and long-term aging is 20 years. A high power output of 15 dBm is available. Pricing starts at less than $70, depending on configuration and volume.

Bliley Technologies, Erie, PA. (814) 838-3571. [www.bliley.com].

Kit Eases FPGA-based Firmware Development

Real-time signal acquisition and processing are critical in applications such as radar, electronic warfare and lidar. Developing such systems depends heavily on data streamer analyzers and signal analyzer cards. Feeding such needs, Acqiris now offers a complete firmware development kit (FDK) that simplifies application development on the embedded FPGA of the company's SC240/210 streamer analyzers and AC240/210 signal analyzers.

Designed to simplify the use of the Virtex II Pro VP70 FPGA, the FDK provides VHDL controllers for all onboard addressable resources. These include the MAC100 Acqiris memory and acquisition controller for data entry, a local bus interface, the DDR SDRAM and dual port SRAM memory controllers, and the front panel I/O controls interface. In addition, a Serial Front Panel Data Port (Serial FPDP) VHDL controller is available for the onboard optical data links on the SC240/210. The FDK design flow supports the major EDA tools from Mentor and Xilinx. A complete test bench comes with text scripts for automated test with ModelSim. Other features include a bit file header insertion with Acqiris' FPGALook software as well as JTAG support for Xilinx ChipScope Pro (integrated logic analyzer) and PowerPC 405 processor emulation. Pricing for the FDK is $18,690.

Acqiris USA, Monroe, NY. (877) 227-4747. [www.acqiris.com].

Low-Power, Fanless Micro PC Features Geode LX800

Military engineers can use a compact, low-power, high-performance micro PC from WIN Enterprises as an entry-level embedded computer. The PL-01030's fanless operation makes it attractive for control applications, and its compact size, at only 8 1/8 in. high, makes it ideal for mobile, in-vehicle applications. It features an AMD Geode 500 MHz LX800 low-power processor, a CS553 chipset and a Dual Winbond 83627HG I/O chipset. The board consumes only 12W from a 5V power supply @ 2.4A. Up to 1 Gbyte of 400 MHz DDR SO-DIMM memory is included, as well as 2-254 Mbytes of AMD Geode LX800 shared system memory that supports a CRT and 24-bit TFT LCD interface.

The PL-01030 has one 50-pin CompactFlash Type II socket and comes with a mounting kit for a 2.5-in. hard drive. For connectivity and expansion, it has two 10/100 Fast Ethernet LAN interfaces, one PC/104 connector, four USB 2.0 ports, four RS-232 ports, one DB-25 parallel port and one DB-25 VGA connector. Audio interface is one mic in and one speaker out. Options include two Intel 82551ER or Realtek 8139CL+ Ethernet controllers. Single unit prices are $392 for the Intel 82551ER LAN version (PL-A1030) and $385 for the Realtek 8139CL+ LAN version (PL-B1030).

WIN Enterprises, N. Andover, MA. (978) 688-2000. [www.win-ent.com].

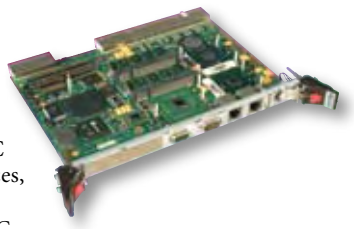
PCI-to-GPIB Controller Card Boasts Low Profile

The GPIB bus ranks high among military system designers as a popular interface solution for linking up larger I/O arrays. ICS Electronics announced a new PCI to GPIB Controller Card for controlling test instruments. Designated the Model 488-LPCI, this new card converts any desktop or portable PC with a PCI bus into a full-function, IEEE 488.2-compatible Bus Controller. The 488-LPCI with its 1 Mbyte per second data rate speeds up data transfers and minimizes test time.

The 488-LPCI Controller is a small, low-profile PCI card that plugs onto any open PCI slot. Because it is a low-profile card, the 488-LPCI can be used with standard desktop PCs and with newer, smaller PCs that take advantage of the space savings resulting from the use of low-profile cards. The 488-LPCI is shipped with a standard PCI bracket and with a spare low-profile bracket. The 488-LPCI comes with ICS's new 488.2V3 Driver Library for Windows 2K, XP and Vista 32-bit operating systems. The 488.2V3 Driver Library supports up to 16 GPIB Controllers and installs a GPIB-32.DLL that is command-compatible with the National Instruments command sets. Pricing for the 488-LPCI is $395 each in quantities of 1 to 4 units.

ICS Electronics, Pleasanton, CA. (925) 416-1000. [www.icselect.com].

cPCI SBC Blends Dual-Core Xeons, 8 Gbyte DRAM



The magic of semiconductor integration has enabled the two-slot SBCs of a couple years ago to now squeeze down to a single slot with equal or more functionality. Such is the case with Concurrent Technologies' latest dual processor 6U CompactPCI SBC, the PP 421/23x, which features two 1.66 GHz Dual-Core Intel Xeon ULV processors. The board is ideal for CPU-intensive processing applications whereby the four processor cores can access up to 8 Gbytes on board DDR2 ECC dual channel SDRAM, whilst maintaining a single-slot solution. For I/O flexibility there is a PMC site supporting both front and rear I/O, two SATA150 interfaces, two graphics interfaces, four Gigabit Ethernet interfaces, PICMG 2.16 (Ethernet switched fabric), PICMG 2.9 (IPMI) and PICMG 2.1 (hot swap).

The front panel also supports a USB 2.0, RS-232, analog graphics, keyboard and mouse interfaces. As well as the PMC rear I/O, the rear panel supports three more USB 2.0, two more RS-232, two SATA150, one EIDE, digital graphics, keyboard and mouse interfaces. Other features included are a watchdog timer, LAN boot firmware and options for an onboard 2.5-inch EIDE hard disk drive and/or CompactFlash EIDE storage. For applications requiring rear I/O connections, a rear transition module is also available.

Concurrent Technologies, Woburn, MA. (781) 933 5900. [www.gocct.com].

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MicroTCA Tower Chassis Is Portable

Over the last several months, MicroTCA has wedged itself into the mindshare of military systems designers. Offering a portable MicroTCA chassis solution, Elma Electronic has announced a new MicroTCA Portable Tower. The Tower features a carrying handle for easy portability. The Type 32M MicroTCA Portable Tower is ideal as a development chassis. Utilizing Elma's modular extrusion-based design, the chassis facilitates a wide rage of configurations. It allows up to 6 AdvancedMCs in the full size format. The modules could be either single- or double-width format in the same backplane.

With two MicroTCA Carrier Hubs (MCH), the backplane has a Dual Star architecture. There are also redundant power modules, connections for two cooling units and M4 power bolts. The MCH slots come in 1-4 tongue styles. The Type 32M features advanced EMC shielding, scratch-resistant vinyl clad aluminum covers and power components. Cooling is achieved with 2 x 90 CFM fans. Elma has performed thermal simulations to ensure the optimal performance. Elma's Type 32M MicroTCA Tower price is under $2,500, depending on volume and options.

Elma Electronic, Fremont, CA. (510) 656-3400. [www.elma.com].

1553 Transformer Is Ready for Rugged Duty

The MIL-STD-1553 bus while far from new, continues to be the interface of choice for reliable, low-latency military control apps. And vendors of 1553 electronics are keeping pace with updated solutions. An example is Beta Transformer Technology's new MIL-STD-1553 dual transformer, the DSS-1000 Series. This new Series is available in ratios compatible with +3.3V, +5V, +12V and +15V transceivers. The DSS Series is suited for designs where both short and long stub ratios are needed within one package and/or a low-profile dual transformer is required.

The DSS Series operates over the full Mil-temp range of -55° to +130°C. This series is also available using tape and reel packaging. The DSS-1000 Series transformers are dual, side-by-side pulse transformers that provide the turns ratio configurations, component isolation and common mode rejection ratio characteristics necessary for MIL-STD-1553 Data Bus specification compliance. These versatile pulse transformers meet all the electrical requirements of Manchester II serial biphase data transmission. To meet the rugged demands of airborne and ground-based military applications, they are encapsulated in accordance with MIL-PRF-21038. Sinusoidal or trapezoidal waveforms are transmitted with minimal distortion, making the DSS Series an excellent choice for any MIL-STD-1553A or B application.

Beta Transformer Technology, Bohemia, NY. (631) 244-7393. [www.bttc-beta.com].

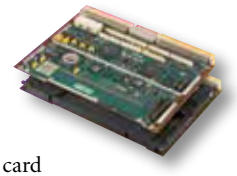
Single-Slot, Multi-Function 3U cPCI Card Packs it All In

Military programs, including airborne, shipboard, ground mobile and C3I applications, are hungry for highly integrated I/O solutions. Feeding such needs, North Atlantic Industries has announced an improved single-slot, 2-module, multi-function, 3U cPCI card. This universal card eliminates the complexity and size constraints of using multiple, independent, single-function cards. The 75C2 cPCI card—which extends the capability of the earlier 75C1—can include the functions of Synchro/Resolver Measurement (4-channels), LVDT Measurement (4-channels), A/D (10-channels), D/A (10-channels), Function Generator (4-channels), Discrete I/O (16-channels), TTL I/O (16-channels), Transceiver I/O (11-channels) and RTD (6-channels).

The interchangeable multi-function design of the 75C2 provides extensive diagnostics and is available in both commercial temperature range and severe environment, industrial temperature range. The library of module types and functions consists of more than sixteen modules and is growing. For increased flexibility, each of the functions of the 75C2 is highly programmable at the channel level. Continuous background (BIT) testing is performed on all functions and channels. The 75C2 is available with operating temperature ranges of -40° to +85°C and 0° to +70°C. Conduction-cooled versions with wedgelocks are also available.

North Atlantic Industries, Bohemia, NY. (631) 567-1100. [www.naii.com].

6U VME SBC Offers High I/O, Low Cost for Rugged Apps



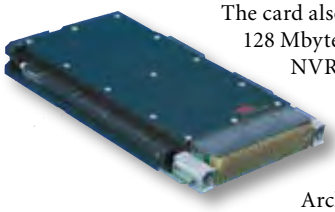
For most military designers, the greater number and types of I/O packed into a single SBC, the better. A new 6U VME SBC from GE Fanuc Embedded Systems, the EP2A, is designed specifically for rugged defense and aerospace applications such as mission computing and communications. It offers a unique I/O set, comprising its four fast HDLC-capable serial ports along with Gigabit Ethernet, USB and GPIO interfaces. Based on a Freescale PowerPC MPC7448 processor, the EP2A is the latest in the company's EmPower family. It features 1 Gbyte of DDR SDRAM and the latest Marvell Discovery V integrated system controller.

Even more flexibility is achieved with two PMC sites as well as GE Fanuc's unique Additional Flexible Interface Xtension (AFIX) card site, which allows designers to add custom functionality quickly and for a low cost. The PMC sites and the AFIX site can be employed simultaneously without sharing I/O pins with the onboard I/O. AFIX cards are available that support dual MIL-STD-1553B interfaces, SCSI, graphics and flash memory. Available in five air- and conduction-cooled environmental levels, the EP2A is supported by comprehensive Deployed Test Software (BIT and BCS) and BSPs for VxWorks, LynxOS and Integrity. Price is $4,800.

GE Fanuc Embedded Systems, Charlottesville, VA. (800) 322-3616. [www.gefanucembedded.com].

SBC Features VPX Benefits for Small 3U Defense Apps

Designers of space- and weight-constrained defense and aerospace systems can reap several benefits from VPX, including high bandwidth, serial switched fabric support and rugged ESD protection. The VPX3-125 from Curtiss-Wright Controls Embedded Computing delivers those benefits and is the company's first VPX SBC in a compact, lightweight 3U form-factor. A VPX-REDI version is also available. The card features the P.A. Semi PWRficient PA6T-1682M, a single- or dual-core, low-power, Power Architecture Platform processor running at 1.5 GHz. This processor is especially well suited for driving new platforms, such as the VPX3-125 SBC, with support for high-speed serial switched interconnects, such as PCI Express and 10 Gigabit Ethernet, with outstanding performance per watt.



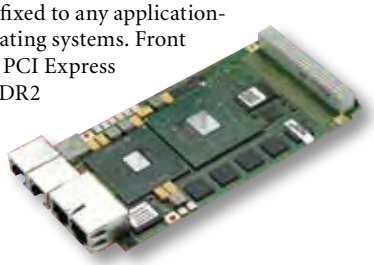
The card also includes 512 Mbytes/1 Gbyte of 400 MHz DDR2 memory, 128 Mbytes of NOR flash, 1 Gbyte of NAND flash and 512 Kbytes of NVRAM. An XMC/PMC site, two x4 lane PCI Express egress ports off board, two 10/100/1000 Ethernet ports, RS-232 and RS-422 serial channels, a USB 2.0 host port and discrete digital I/O are provided for connectivity and expansion. The VPX3-125 conforms to Curtiss-Wright's Continuum Software Architecture (CSA) interoperability initiative. Drivers for VxWorks/Tornado 6.x and Linux are included. Pricing starts at $6,919.

Curtiss-Wright Controls Embedded Computing, Leesburg, VA, (703) 779-7800. [www.cwcembedded.com].

Embedded Module Serves Up 1.67 GHz Core Duo

The Intel Core Duo seems to be usurping the Pentium M's position as the most widely used processor on new embedded board products. The processor fits nicely into the increasing demand for high compute density in military applications like UAV payloads. Along just those lines, MEN Micro has announced another ESM Embedded System Module—the EM6, based on Intel's 1.67 GHz Core Duo—or alternatively Celeron M processor—and the Intel 3100 chipset, the EM6. Combined with Altera's Cyclone FPGA, the board is much more flexible than traditional PCs as the required system I/O can be realized individually for each application using IP cores.

ESM modules are complete computers on a plug-on module. They consist of the hardware (CPU, chip set, memory); board-specific I/O; an FPGA, which is not fixed to any application-specific function and board support packages for various operating systems. Front I/O of the module comprises two Gbit Ethernet controlled via PCI Express as well as two COM interfaces via RJ45 connectors. The fast DDR2 SDRAM memory comes in directly soldered on the EM6 against shock and vibration. The also soldered-on 1 Gbyte flash memory can replace a rotating mass storage device in many applications.



MEN Micro, Ambler, PA. (215) 542-9575. [www.menmicro.com].

SDR Server Links Ethernet to Legacy RS-232 Devices

EOIP (Everything-Over-IP) has become the rallying cry for the military's effort to migrate to completely net-centric operations. But linking those IP-based networks with legacy serial devices is an important piece of that puzzle. RS-232 Legacy Devices are now IP addressable with the Lexycom Technologies software defined radio. The latest version of firmware for the Tiamis-800 software defined radio transceiver (SDR) allows legacy RS-232 serial equipment to be connected to Ethernet. The Tiamis-800 is a fully digital, user-programmable data transceiver that uses frequency hopping spread spectrum technology. With adjustable RF channel data communication speeds of up to 1 Mbit/s and user selectable frequency channels, the Tiamis-800 is able to provide fast, secure and reliable wireless communications even in the most complex environments.

With this feature serial—RS-232, RS-422 or RS-485—devices can be wirelessly connected to an Ethernet network. Lexycom's wireless Ethernet-to-Serial Server handles all required protocol conversions and allows the user to add IP addressing capability to their legacy serial devices. System designers and network users are now able to realize the maximum benefits of their existing infrastructure by taking full advantage of the IP-based network's capabilities.

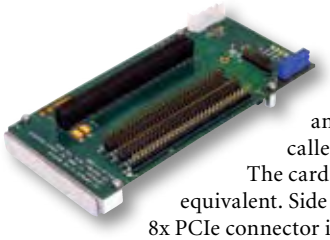
Lexycom Technologies, Longmont, CO. (303) 774-7822. [www.lexycominc.com].

CompactPCI Board Sports Dual 1.4 GHz PowerPCs

CompactPCI has passed the test of longevity and maturity, making it one of the accepted form-factors in today's military applications. Feeding that trend, Interface Concept has unveiled a high performance 6U CompactPCI board, the IC-xe6-cPCIb, powered by one or two Freescale 1.4 GHz MPC7448 PowerPC processors. This new single or dual processor SBC is PICMG2.16-compliant and blends low power consumption and large communications capabilities. The board implements a Marvell Discovery III chipset (MV64460).

The memory banks are made of up to 2 Gbytes of DDR-ECC SDRAM, up to 256 Mbytes of mirror flash and up to 1 Gbyte of soldered NAND flash. A quad UART provides four additional asynchronous channels available on P2 connector. The 64-bit PCI/PCI-X bridge allows the IC-xe6-cPCIb to handle two PMC slots with PnIO routed to J3/J5. Thanks to its SATA controller, the IC-xe6-cPCIb can manage directly four storage devices. The IC-e6-cPCIb provides one Gbit Ethernet, one console, one USB-2 and two SATA ports on the front panel. This board has been designed to meet the most severe environments—standard, extended and rugged grades. Prices start at $3 950.

Interface Concept, Briec de l'Odet, France. +33 (0) 298 577 176. [www.interfaceconcept.com].



Adapter Card Facilitates PCIe to XMC Migration

The broad proliferation of PCI Express (PCIe) and the ruggedness of XMC mezzanine form-factor together make an ideal recipe for migrating functionality from one to the other. Fueling such efforts, Technobox has introduced an XMC card that facilitates the development of XMC cards and/or related software. Using the PCIe-to-XMC Adapter, called the 4876, an engineer can adapt an existing PCIe solution to an XMC site on a carrier or single board computer.

The card is an especially useful tool for software development where an existing PCIe solution is to be ported to an XMC equivalent. Side one of the 4876 has a pair of XMC connectors for the P15 and P16 interfaces that mate with the host XMC site. A single 8x PCIe connector is located on the opposite side of the adapter, along with some headers and jumpers. Two 64-pin headers are provided to permit probing of various XMC signals from the P15 and P16 connectors. Pin assignments conform to VITA 42.0-2005 and VITA 42.10-200x. Onboard LEDs provide indication of key XMC signals and power status. The adapter is equipped with a connector to accept external +12 volt power. The 4876 is priced at $895.

Technobox, Lumberton, NJ. (609) 267-8988. [www.technobox.com].

Mini-ETX Motherboard Aimed at Rugged, Low-Power Computing

A new motherboard based on the mini-ETX form-factor and featuring HDTV output is targeted at defense and aerospace applications that require ruggedization and low power consumption. The Mini-ITX-9452 from Arista features the Intel Core Duo/Core Solo processor, dual PCI Express Gigabit Ethernet, HDTV output and two independent audio streams. It is equipped with a Socket 479 Intel Core Duo/Solo with a 667 MHz FSB and an Intel 945GM chipset + ICH7M. System memory includes two 240-pin dual-channel memory slots that accommodate up to 2 Gbytes of DDR2-400/533/667 RAM.

The motherboard requires a low, 1.58-amp, 5V maximum power and has a programmable watchdog. Additional features include eight USB 2.0 ports, two SATA II AII-300 ports, a PCI slot, a mini-PCI slot and ATX support. Integrated Intel 945GM support and dual 18-channel LVDS and CRT are included. Pricing starts at $380.

Arista, Fremont, CA. (510) 226-1800. [www.aristaipc.com].

USB I/O Module Dressed for Rugged Roles

While slow to find a place for itself in embedded applications—and even slower to do so in embedded military systems—Universal Serial Bus (USB) has begun to see acceptance in both those arenas. Serving such needs, Advantech has introduced the USB-4716, a 200 ksample/s 16-bit multi-function USB I/O module. The USB-4716 has been specifically designed for rugged environments and includes a USB connector with screw fasteners and a DIN-rail mounting kit. It draws power directly from the USB port and therefore does not require an external power supply. The USB-4716 is packed full of I/O ports, including 16x single-ended (8x differential), 16-bit 200 kS/s analog inputs, 2x 16-bit analog outputs, 8x digit inputs, 8x digital outputs and 1x 32-bit event counter.

The USB-4716 comes with WaveScan, an easy to use trending and data logging software program. In addition to WaveScan, Windows APIs, Active X controls and LabView drivers are included. This allows programmers easy interface for application development like data logging, test stand data acquisition, waveform analysis and mobile measurement applications. The device is priced starting at $650.

Advantech, eAutomation Group, Cincinnati, OH. (513) 742-8895. [www.eAutomationPro.com].

Board Does Wide-Band Sensor I/O Over Ethernet

The military has warmed completely to the idea of using Ethernet as high-performance interconnect technology. Its ubiquity and longevity make it hard to resist. Applying Ethernet to wide-band sensor I/O, Critical I/O has announced SensorLink, a board-level solution that allows wide-band sensors to be easily connected to, and managed over, 1 Gbit and 10 Gbit Ethernet networks. SensorLink enables the world's first Ethernet "Sensor Fabric" for high-performance systems.

With SensorLink, Ethernet data networks can be applied to even the most demanding real-time applications such as radar, data acquisition, sonar, FLIR, SIGINT, video distribution and signal processing. Completely self-contained and requiring no host processor, SensorLink allows sensor data to be streamed at wire speed with very low latency to other devices connected to the Ethernet network such as signal processors, workstations, storage devices or other SensorLink devices. SensorLink also greatly simplifies the management of sensors by allowing remote processors to configure, control and monitor them through the same Ethernet connection without interrupting the sensor's real-time data flow. SensorLink allows system developers to directly leverage standard Ethernet networks without investing many man-years in software and compatibility testing.

Critical I/O, Irvine, CA. (949) 553-2200. [www.criticalio.com].

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COTS View

Virtualized Strategy Smooths Military System Development

Gone are the days when software comprised a minor part of system functionality. In today's military systems software design and system design are one and the same.

Paul McLellan, Vice President of Marketing
Virtutech

Over the past few decades, the number of lines of code in a typical military electronic system has increased a hundredfold. Take, for example, a 1960s-era jet fighter, which contained roughly 50,000 lines of code. By contrast, today's modern-era stealth fighter can demand upward of five million, and more than 80 percent of its functionality is software-based.

These numbers point to the dramatic shift that has taken place in the makeup of military electronic systems over time (Table 1). Historically, software comprised a smaller, less significant portion of a given system, with much of the functionality tied to hardware. Consequently, hardware design absorbed much of the focus of system developers, and software was treated as a secondary concern. According to

Figure 1
General Dynamics C4 Systems utilizes virtual models of satellite hardware in emulation routines implemented by the NASA Gamma-Ray Large Area Telescope (GLAST) mission operations center. As the hardware simulation can be configured on a PC without any modifications to the physical hardware, a range of failures and irregularities can be easily and repeatedly injected without risk of damage to expensive hardware.

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Electronic Systems: Then and Now

Then	Now
Hardware was a dominant component of system design	System design dominated by software
Performance increase though increased clock speed	Performance increase throgh additional core
Could leave software until the end of development	Software development must start early
Hardware-based methodology effective	Hardware-based methodologies running into the wall

Table 1

A dramatic shift has taken place in the makeup of military electronic systems over time. Today it's more convenient and cost-effective to achieve system differentiation and functionality through software.

The military is no stranger to virtualization. In many respects, the military industry has been ahead of the curve, employing simulation technology for advanced design and training purposes.

Moore's Law, however, semiconductor speed has increased, making it more convenient and cost-effective to achieve system differentiation and functionality through software. As a result, military electronics has witnessed explosive growth in the size and complexity of software components.

Over the past 20 years, hardware productivity has increased by a factor of 10,000 due to heavy investment in hardware design tools by electronic design automation (EDA) companies. Without a comparable level of investment in software development tools, the average productivity of programmers has increased by a mere factor of 10 over the same amount of time. As the software in military systems continues to rise in complexity, particularly with the advent of multicore architectures, and as additional mission-critical functionality comes to be dependent on software, developers must look to software design tools that break from traditional development methodologies.

Virtualization as a Development Tool

Virtualized software development is one innovative approach that has the potential to address the divergence between increasing software complexity and relatively static programmer productivity. By virtualizing software development, engineers are no longer dependent on executing software on physical hardware, instead performing the test, development and debug process on a more flexible, controllable virtual model.

The military is no stranger to virtualization. In many respects, the military industry has been ahead of the curve, employing simulation technology for advanced design and training purposes. The use of virtualization in the software development realm, however, has not become a mainstream practice, in part due to the assumption that simulation, as evidenced by lower-level simulators such as Spice or Verilog, is far too slow to accommodate a developer's edit-compile-debug cycle.

The application of virtual hardware models extends beyond software development processes into training processes, making virtualization technology a powerful tool for military applications requiring rigorous end-user and operator training and evaluation. Responsible for designing and building the NASA Gamma-Ray Large Area Telescope (GLAST) spacecraft (Figure 1), General Dynamics C4 Systems utilizes virtual models of satellite hardware in emulation routines implemented by the GLAST mission operations center. As the hardware simulation can be configured on a PC without any modifications to the physical hardware, a range of failures and irregularities can be easily and repeatedly injected without risk of damage to expensive hardware. This flexible environment enables the mission operations team to implement training exercises that will aid in recognition of and response to in-orbit failures.

The Edit-Compile-Debug Loop

Recent advancements in virtualization technology, such as just-in-time compilation (JIT) and acceleration of idle time,

By modeling I/O accesses as single, synchronous events, the simulator can rapidly simulate processor workloads using the real operating system, network protocol stacks and the actual application code.

along with fast and inexpensive workstations, allow complex systems to be modeled at speeds measured in billions of simulated instructions per second. This level of performance makes virtualization a very viable tool for the edit-compile-debug loop that comprises a large part of a programmer's daily workload.

The technology underlying virtualized software development achieves a level of accuracy that enables production binaries to run unchanged and at very high performance. The simulator is event-driven. It models and analyzes communication at the transaction level, thus eliminating the need to use actual, bit-level bus traffic. By modeling I/O accesses as single, synchronous events, the simulator can rapidly simulate processor workloads using the real operating system, network protocol stacks and the actual application code.

The simulator relies on a single global virtual time base, which synchronizes all processors and other devices, allowing developers to halt the whole system simulation when one part of the system is stopped. This advanced capability is particularly important given the upcoming wave of multiprocessor and multicore systems. The single-step operation serves as the key to deterministic debugging. Due to the fact that every system node is observable and traceable, and its state and behavior over virtual time can be logged, system tracing can be used to comprehensively profile the software and perform code coverage analysis. Also, due to the behavioral model's high level of abstraction, there is no strict limit to the number of processor cores—with homogenous or heterogeneous operating systems—executing in parallel that the simulator can run, analyze and debug. Complete systems with hundreds and even thousands of processor can be successfully modeled.

Running Code Both Ways

Virtualization also rewrites the standard rule that code can only run forward. When an error occurs while running code on physical hardware, developers must engage in the time-consuming process of rebooting the system from the be-

Benefits of Virtualized Software Development	
Determinism	Always get the same result when re-running a test, even on multiprocessor systems
Binary Compatibility	Run the real production binary, even device drivers and operating systems
Speed	Run real-world workloads and use for all debugging
Hindsight	Can run code backwards to search for deep errors
Hypersimulation	Can skip idle code to handle very large multiprocessor systems effectively
Non-invasive	Can observe anything in the system non-intrusively

Table 2

With the ability to execute code in reverse, virtualization makes it possible to wait for an error to occur and then run backward to determine the root cause, providing significant debugging benefits over physical hardware.

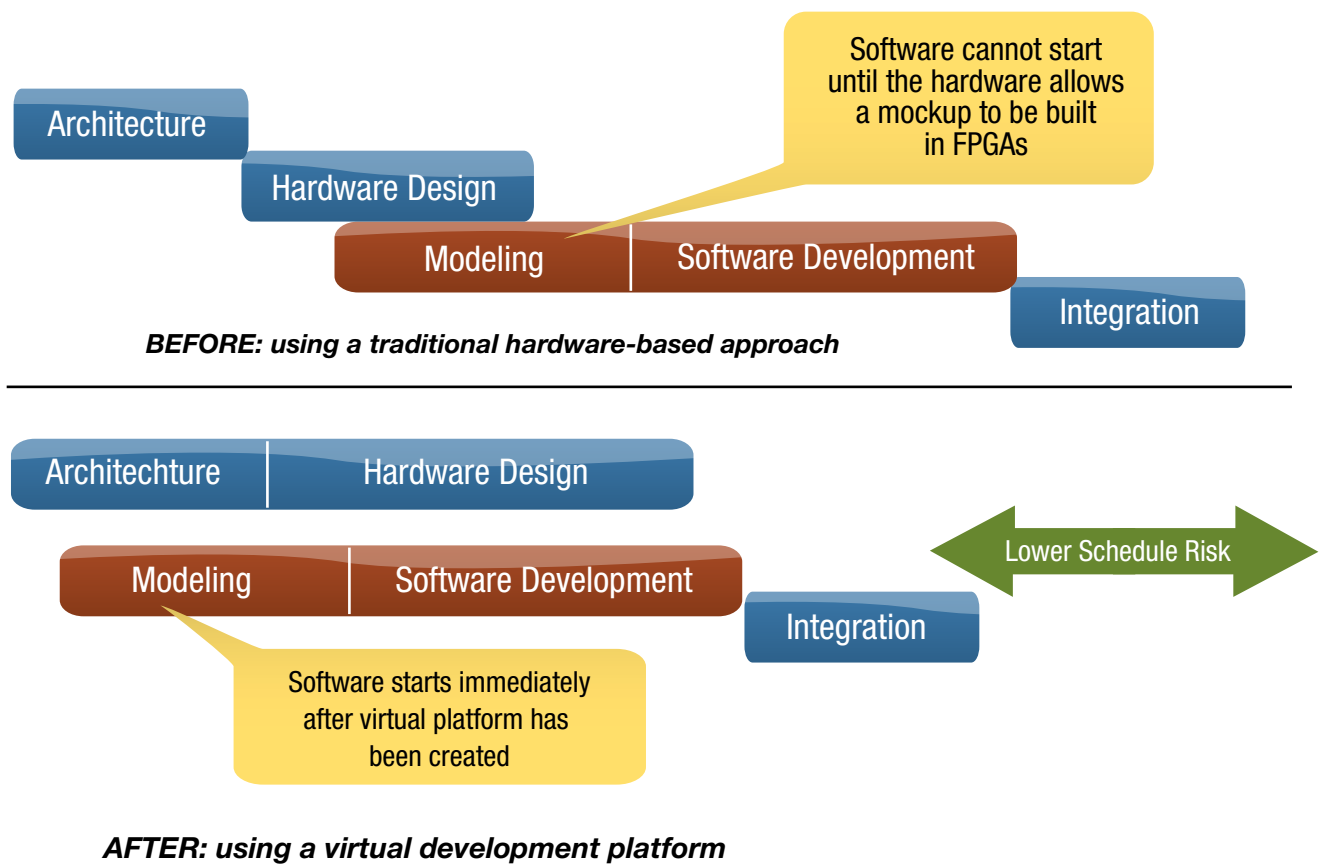

Figure 2

Using virtualization, software defects can be found and resolved earlier during the development phase instead of the system integration phase. This approach yields higher quality code, time savings and lower development costs.

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ginning and re-running it to the point just before that particular procedure call, with no guarantee that the bug can be reproduced. With the ability to execute code in reverse, virtualization makes it possible to wait for an error to occur and then run backward to determine the root cause, providing significant debugging benefits over physical hardware. Simulation has the ability to reverse the entire system, even disks, network devices, multiple processors and terminals, and is effective with operating-system crashes, segmentation faults and accidental file deletions (Table 3).

Virtualization in Practice

Due to the nature of military system operations, the military segment has proven to be an area that is ripe for virtualization technology, and developers have begun to make the shift from executing software development on hardware to utilizing a virtualized software development approach. While military electronic systems do not face the typical time-to-market pressures found in consumer electronic systems, the amount of mission-critical functionality controlled by software translates into more stringent quality and documentation standards.

In addition, as part of a very large overall program, individual schedules can have huge knock-on effects if they are missed. Virtualized software development has enormous potential to meet these standards, not only due to the increased programmer productivity that it supports, but also because of the ability to proceed concurrently with hardware and software design. As software defects can be found and resolved earlier during the development phase instead of the system integration phase, the approach yields higher quality code, time savings and lower development costs (Figure 4).

BAE Systems currently utilizes virtualization technology in the development of space-bound applications on the RAD750 Space Computer, BAE Systems' third-generation space processor. With more than 300 MIPs, the RAD750 provides nearly 10 times the performance of current space processors.

BAE Systems' customers using the RAD750, such as Smiths Aerospace, can employ a virtual model of the processor to begin software development years ahead of flight hardware availability, enabling early development, benchmarking and testing of the software, as well as testing and evaluation of critical failure mechanisms. Because these operations offer little margin for error in both system quality and timetables for launch, developing software in parallel with the hardware design and prototype bug represents significant reduction of both schedule risk and cost.

In the case of the Northrop Grumman Corporation's Navigation Systems Division, virtualized software development has been employed in a pilot project involving software development and testing for selected navigation systems. Northrop Grumman simulates its navigation systems and customizes its software for a variety of applications, providing the opportunity to evaluate and test how newly created software will operate. This move toward a virtualized development approach will help validate software modifications and speed completion of the project.

Coping With Multicore and High-Density Computing

With the expected proliferation of multicore architectures and the continuing move toward high-demand, compute-intensive military systems, software developers face a mounting challenge that renders traditional, hardware-based development techniques inadequate. Virtualized software development is the only approach that enables developers to begin earlier in the production cycle, prior to hardware availability, offering both cost- and time-saving advantages that have become increasingly critical in military electronics.

In contrast to hardware-based approaches, virtualization offers an unparalleled level of system-wide controllability, insight and determinism that is necessary to resolve the development challenges presented by multicore and truly concurrent environments. As virtualized software development encounters wider adoption, the military industry will undoubtedly benefit from more precise, higher quality embedded systems that are imperative for modern mission-critical applications. ▮▮

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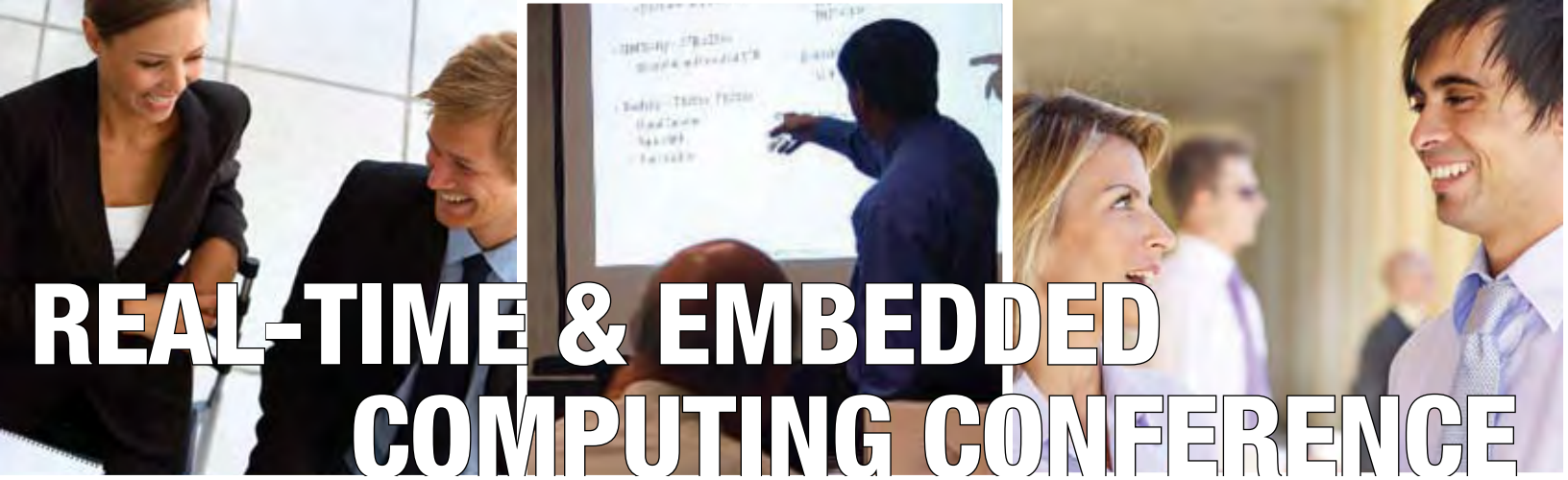
Coming Next Month

COTS JOURNAL

- FPGAs and Reconfigurable Computer Boards. As the signal processing capabilities of FPGAs continue to climb, board-level reconfigurable computing solutions have grown to become the key enablers for waveform-intensive applications like sonar, radar, SIGINT and SDR. Such systems have an insatiable appetite for more digital signal processing muscle. This feature section delves into the solutions available in reconfigurable computing and how they're transforming military signal processing systems.
- Next-Generation VME. This is shaping up to be the year that VITA 46—now called VPX—will move to more than just concepts and prototype products. Expect several vendors to roll out VPX board, chassis and backplane products this year. This section updates readers and the latest spec and product developments in both VPX and VXS (VITA 41), and analyzes where these architectures are positioned these days among the various form-factors available to today's military system designers
- MILS and Information Assurance. You'll find the term Information Assurance (IA) part of any discussion about today's network-centric programs like FCS, WIN-T and JTRS. The information and databases on the military's networks are national assets, and enemy access to them threatens our warfighters. To ensure security in these systems, developers are leveraging architectures like MILS (Multiple Independent Levels of Security). This section examines the embedded OS and hardware building blocks central to MILS and IA.
- PXI,VXI and LXI Boards. For complex, high-performance military systems, the PXI bus form-factor, and its older cousin VXI, have become staples as instrumentation and test solutions. Now the LAN-based LXI form-factor is the latest stepchild in this space to emerge on the scene. This Tech Focus section updates readers on the latest trends in these technologies along with a focused product album of representative boards in these architectures.



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COTS

Editorial

Jeff Child, Editor-in-Chief

The Stumble Before the Finish Line

Earlier this month my *COTS Journal* colleagues and I made our annual trek to the Association of the U.S. Army (AUSA) show down in sunny Ft. Lauderdale—it wasn't hard to drag me away from my New England offices during the frigid cold of early March. AUSA never fails to provide me a clear sense of the state of Army and Joint programs—particularly those fueled by embedded computing and communications technology. Moreover, the time of year—coming on the heels of the annual DoD budget proposals—lets me look at programs in context of what their funding situation looks like.

At AUSA, I was struck with how far—compared to three or four years ago—programs like JTRS, FCS, WIN-T and Land Warrior have advanced. A couple years ago those programs were still in a very conceptual and planning stage, with far more technical and organizational challenges ahead of them than behind them. Fast-forward to today, and it's clear that those major advanced technology programs have really come together and are getting close to the "real deliverables" stage.

Last month in this column, I talked about the Army's Land Warrior program falling victim to budget cuts. The poor weight and battery life of the Land Warrior wearable computing system were among the reasons for the program termination. In spite of that, it was clear from what I saw at AUSA that solider-wearable computing is alive and well. Last fall General Dynamics C4 Systems launched an initiative called the EDGE, which is intended to speed the delivery cycle of systems worn and carried by warfighters. The initiative combines industry, government and academia including Arizona State University's Flexible Display Center. At their booth at AUSA, General Dynamics was showing a soldier-wearable computing system that integrated three separate modules of the Land Warrior system down into a single module.

Meanwhile, the Future Combat Systems (FCS) program, in contrast to past years at AUSA, has clearly emerged into something you can see, hear and touch. At AUSA, General Dynamics C4 Systems and Rockwell Collins were showing off at their booths the first FCS ICS. The week of the show, the firms announced the delivery (on schedule) of the first ICS to the U.S. Army's FCS program. ICS is the common computing environment for most of the platforms in the FCS program family of systems, which comprises sensors, UAVs and manned and unmanned ground platforms.

Called the Large Networking Processor, this first ICS provides computing, networking and information assurance resources to enable U.S. Army current force vehicles to be a part of the FCS network. The system is based on 3U CompactPCI cards with Pentium M computing and 10-port Gbit Ethernet switching. Bradley fighting vehicles, Abrams main battle tanks and Command-Variant Humvees are scheduled to be equipped with ICS as part of the first spin-out of FCS future force technologies in 2008.

Along related lines, BAE Systems was likewise showing off FCS gear in their AUSA booth, including its Bradley Technology Demonstrator (TD). The Bradley TD is BAE Systems' look at managing the Bradley Combat Systems into the future. Among the Demonstrator's features were Remote Turret operation, Panoramic Vision, Embedded Diagnostics, Embedded Training system and an FCS Spin Out One mock-up.

Also at AUSA, the FCS program booth was showing great video footage of the FCS Experiment 1.1, which ran in three phases from last July 2006 to February 2007 at the White Sands Missile Range, NM and other locations. The field experiment included tests of Non-Line-of-Sight Launch System networking, JTRS Ground Mobile Radio performance and other systems. In the Experiment 1.1 operations, the FCS software ran on a mobile workstation because the Integrated Computer System (ICS) was not yet available.

The final phase of the White Sands field test involved 36 soldier participants who provided "hands-on" feedback of early FCS prototypes. The soldiers drilled in a live training environment using an FCS computer-based training support package. Commenting in the video, the participating soldiers expressed genuine praise for the tremendous advantages the networked situational awareness FCS provided during the operation.

Despite all the positive progress demonstrated by FCS, many of the participating suppliers I spoke to at AUSA expressed concerns that the program will be the target of further budget cuts. With total expected overall lifetime cost exceeding $120 billion for the program, it's ranked among the military's most expensive programs. In the 2008 budget proposal, the FCS program already lost funding for two of its classes of UAVs, and one of its unmanned ground systems has been nixed from the program, along with the Intelligent Munition System.

With a general political sentiment growing in Congress against the idea of spending for technology-intensive military programs, I wouldn't be surprised to see future trimming down of the FCS program. At the stage the program is at, one vendor told, it would be extremely wasteful to break it apart to where some elements would have be developed later. It's the hardware/software commonality of the various FCS platforms that make them suited for development in parallel with one another. It would be a shame if lack of funding causes all the impressive modernization of the Army I saw at AUSA to stumble before it reaches the finish line. ▮▮

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